

Port Nullification, a New Methodology to Simulate Circuits with Nonlinear Devices

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Abstract—A new methodology is presented in this article for finding the dc operating points of nonlinear devices. The method is built around the concept of additivity that has been widely used in linear circuits. This method allows the circuit designer to select a scheme of applying dc (or ac) sources in multiple steps to better control the dc operation of the circuit and get faster convergence. The method is first developed for one-port networks, and then extended to include multiple-port networks. An example of a two stage feedback amplifier is carried out to demonstrate the procedure.

Index Terms— analog_circuits, circuit_analysis, circuit_simulation, nonlinear_circuits, DC_operating_points

I. INTRODUCTION

ALLOCATING the dc operating points (OPs) of nonlinear devices in a circuit is important for the design of analog circuits. However, the job becomes difficult and often complicated for sizable circuits, particularly those with positive feedbacks where the chance for the OP being unstable is quite high. In some advanced circuit simulators, such as SPICE [1], methods based on Newton-Raphson iteration techniques are typically employed. But the major difficulties in these methods are circuit convergence, and the number of iterations that is required to get close enough to the desired OPs. The problem usually arises from applying the entire dc sources at once and with a poor selection of the initial conditions for the OPs. Large and unregulated steps in search for OPs increase the chances of going out of range, and ultimately ending with non-convergence situation [2 - 9].

What we present here is a procedure that allows controlling the search for OPs, and with a more gradual manner. It enables the circuit designer to select different regimes of applying supply sources (dc and ac) to a nonlinear circuit in order to achieve a quick convergence. In this technique, the designer groups the supplies, prioritizes them and applies them in a manner that leads to desired OPs. In short, with this technique the circuit designer has tremendous power to control the nonlinear behavior of the circuit by adopting a *supply sequencing* that even makes it possible to split dc sources, group them, and do different combinations that lead to less iterations and quick convergence.

The idea of “*divide and conquer*” works here!! The key concept that makes all this possible is the additivity property, widely used in linear circuits [10], the only difference here is conditioning the ports for the next step. The way it is done is to record (store) the partial OPs that are found in each

operation and use them as the starting points (the origins of the nonlinear i-v characteristics) for the next operation. This continues until all sources are used and the final OPs are gradually moved to their destinations. The method uses two close concepts: i) *Port Nullification*, and ii) *Network Inactivation*, as will be discussed.

Assumptions and definitions

For simplicity we consider the following assumptions and definitions all throughout the article, unless otherwise stated:

- Networks are assumed to be memoryless (no capacitance or inductance), and they can be nonlinear
- The term *powerless* or *no internal power* is referred to a network that all its independent sources are zero, and its dependency to external signals is also zero.
- A *null* network is referred to a network with no element; leaving the port nodes either open circuited or coalesced.
- A Port $j(v_j, i_j)$ with current i_j and voltage v_j , is augmented by a current source I and a voltage source V if i) a current source I is added across the port, and ii) a voltage source V is added in series with the port, as shown in Fig. 1. Port $k(v_k, i_k)$ is created as the result.

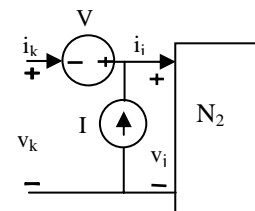


Fig. 1 - Port $j(v_j, i_j)$ of N_2 , augmented to create another Port $k(v_k, i_k)$

Section II of this paper deal with port nullification in one-port networks, and an example is given to clarify the subject. The extension of port nullification leading to network inactivation for multiple-port networks is covered in Section III. In Section IV the implementation of the method on semiconductor devices is discussed, and an example of a BJT feedback amplifier using the nullification technique is worked out.

II. ONE-PORT NETWORKS

Null Port: Consider a network N_2 connected to another network N_1 through a Port $j(v_j, i_j)$, as shown in Fig. 2. Port j is *null* if both i_j and v_j are zero. Note that N_1 can be a null network.

Property 1: In a given network if a port is null then a) the $i-v$ characteristic curve of the port passes through the origin, and b) the origin is the OP for that port.

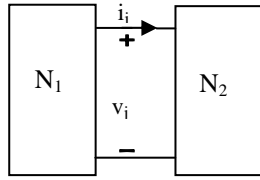


Fig. 2 - A null port representation

Example 1: Consider the circuit of Fig. 3(a), where two parts of a circuit are connected through a Port $j(v_j, i_j)$. Suppose the MOS diode M1 is characterized by $i = K(v-1)^2$ mA, for $v > 1V$, where $K = 0.5$ mA/V². The analysis shows that Port j is not definitely a null port, since $I_j = 1$ mA and $V_j = 3$ V. Next, we augment Port j by current and voltage sources I_j and V_j , from both sides, to create Port $k(v_k, i_k)$, as shown in Fig. 3(b). Now, Port k becomes null since both I_k and V_k are zero. Note that, although the $i-v$ characteristic curve for Port j does not pass through the origin but that of Port k does. It is important to note that Port k is also a port of network N_1 , on the left hand side, and hence its characteristic curve must pass through the origin (Property 1). This simply means that, the (Thevenin or Norton) equivalent circuit of N_1 , looking from Port k , can only be resistive with no source, i.e., we can remove all sources from N_1 with no effect on N_2 , as shown in Fig. 3(c). This leads to Property 2.

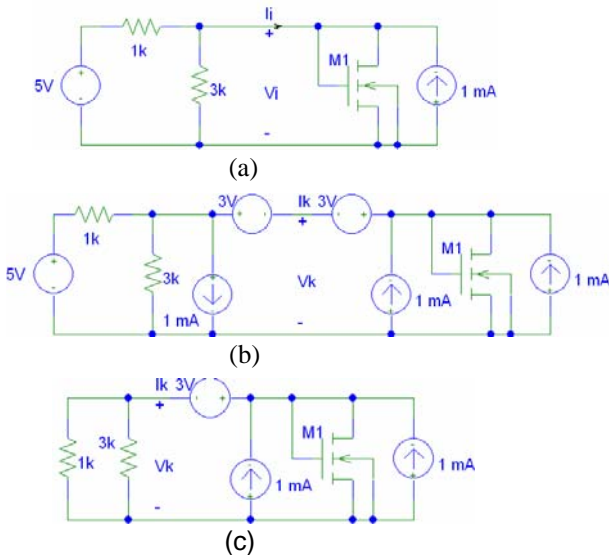


Fig. 3 – (a) Two networks N_1 and N_2 separated by Port j , (b) creation of null Port k , (c) simplified null Port k

Property 2: Consider a network N_2 connected to another network N_1 through a single Port j . If Port j is null then all sources in N_1 can be removed without affecting N_2 .

The proof of Property 2 is evident, because the only source of power to N_1 can be through Port j . But being a null port, Port j cannot transfer any signal (v or i) from N_2 to N_1 . Hence, all currents and voltages in N_1 remain zero, and cannot influence N_2 . The converse, however, is not necessarily true,

i.e., N_1 can have sources while Port j is still a null port, as we notice in Example 1.

Port Nullification: Consider a network N_2 , connected to another network N_1 through a Port $j(V_j, I_j)$, as shown in Fig. 2. Port j is gone through *nullification* if it is augmented, from both sides (N_1 and N_2), by a current source I_j and a voltage source V_j , as depicted in Fig. 4. The result is the creation of another Port $k(V_k, I_k)$ that, by definition, is a null port.

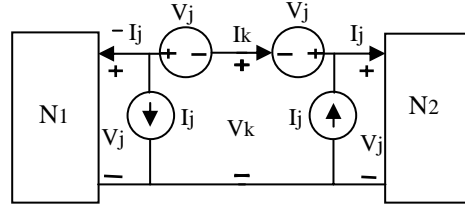


Fig. 4 - Port Nullification procedure

Property 3: Consider a network N_2 , connected to another network N_1 through a Port $j(V_j, I_j)$. Port j is gone through *nullification* if i) all signal sources (dc and ac) in N_1 are removed, and ii) Port j of N_2 is augmented with sources I_j and V_j , as specified in Fig. 5.

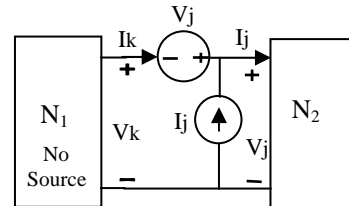


Fig. 5 – An alternate Port Nullification procedure

The proof of Property 3 follows from the definition of *Port Nullification* and Property 2. Note that neither networks, N_1 nor N_2 , needs to be linear.

As specified, a null port may look like a closed *gate* between two networks, N_1 and N_2 , with no exchange of signals happening between them. But this is not exactly true. What is happening is that, for the *existing* situation, i.e., the sources available in N_1 and N_2 , both networks remain in equilibrium conditions and no power is exchanged between them. But if there are some changes (in sources or other components) in either network then the equilibrium may no longer persist. In addition, since null port is a port with zero current and zero voltage then, in lo of Property 3, replacing one network, say N_1 , with another powerless network, including a null network, does not affect the situation inside the other. This brings us to the next property.

Property 4: If a null port is the sole connection between two networks then replacing either network with a powerless network, including a null network, does not affect the other one.

Theorem 1: Consider a one-port network N_2 with its port characteristic curve given in Figs. 6(a) and (b), and let $Q(V, I)$ be a point on the port's characteristic curve. A newly generated Port $k(V_k, I_k)$, connecting N_2 to a powerless network N_1 , is nullified if Port $j(V_j, I_j)$ is augmented by a current source I and a voltage source V , as shown in Fig. 6(c).

The proof of Theorem 1 follows directly from the definition of *Port Nullification*. It is also evident from Property 1 that

both Ports j and k have the same i - v characteristic curve, except that in the case of Port k the coordinates have moved to a new position with Q point being the origin, as indicated in Fig. 6(d).

Now, if we add (power) sources to N_1 , then N_1 runs N_2 , through Port k , as if N_2 has the i - v characteristic curve given in Fig. 6(d). This leads to the next important theorem.

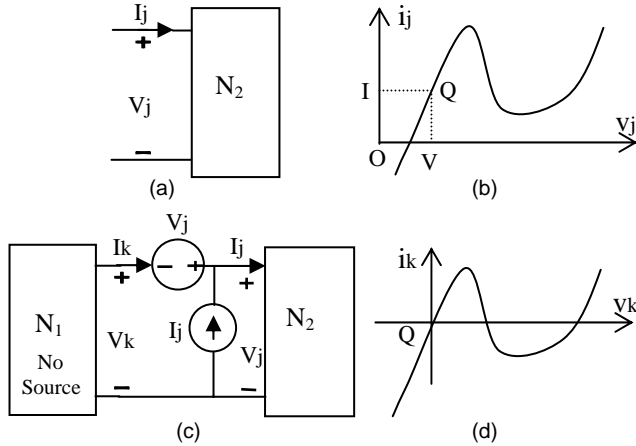


Fig. 6 - (a, b) A one-port network with its port characteristic, (c, d) Port k after being nullified

Theorem 2 - Additivity: Consider a one-port network N_2 , connected to another network N_1 , and let N_1 contain n sources. Group the sources in N_1 into m mutually exclusive groups. Then the total effect of network N_1 on N_2 , due to all n sources in N_1 , can be determined by adding m times the effect of N_1 on N_2 , where a) each time a different group of sources is used in N_1 , and b) the port is nullified before each time the operation is performed.

Proof: Suppose N_1 has n power sources (dc and/or ac) that runs N_2 through Port 1 (v_1, i_1) to an OP $Q(V, I)$, as shown in Figs. 7(a) and (b). Next, split n sources into m groups of sources n_1, n_2, \dots , and n_m . First keep n_1 group of sources in N_1 and remove the rest. Evidently, the OP moves to a new point $Q_1(V_1, I_1)$ on the characteristic curve, as indicated in Figs. 7(c) and (d). Next we augment Port 1 with I_1 and V_1 to create a nullified Port 2 (V_2, I_2). Further, we remove n_1 sources from N_1 and add the group of n_2 sources to N_1 , shown in Fig. 7(e). This new setting moves the OP to $Q_2(V_2, I_2)$, [Fig. 7(f)]. Likewise, we need to augment Port 2 with I_2 and V_2 to create a nullified Port 3 (V_3, I_3), [Fig. 7(g)]. Similarly, remove n_2 and add n_3 group of sources to N_1 . By Property 1, the characteristic curve of Port 3 passes through Q_2 , but the new OP has moved to $Q_3(V_3, I_3)$. This is due to n_3 group of sources [Fig. 7(h)]. For simplicity, suppose the sources in N_1 are exhausted at this point, then Q_3 and Q must be the same points on the characteristic curve. This simply means that $V = V_1 + V_2 + V_3$, and $I = I_1 + I_2 + I_3$, as we can examine in Fig. 7(g).

This proves the theorem for the port situation in N_2 . But the proof can be extended to any other internal signal in N_2 , as well. This is because, any element in N_2 can be considered as a one-port conned to the main network. This proves the theorem.

III. MULTI-PORT NETWORKS

Inactivated Network: Consider a network N_2 connected to another network N_1 through m ports. Network N_2 is *Inactivated* if all m ports of N_2 are augmented (see the procedure) such that the removal of all of the sources in N_1 does not affect the internal conditions (voltages and currents) in N_2 .

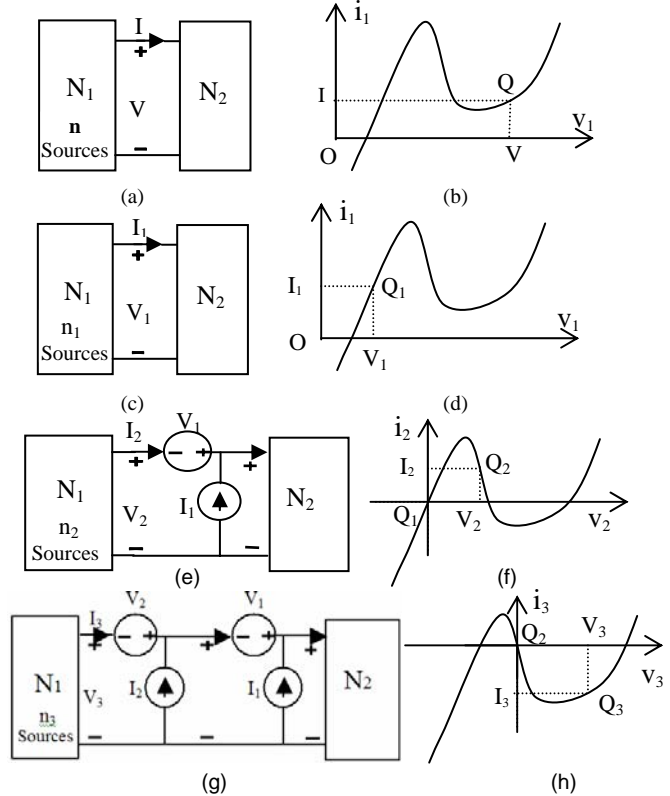


Fig. 7 – Additivity Property, and steps in supply sequencing

Theorem 3: Consider a network N_2 connected to another network N_1 through m ports. Nullify all m ports of N_2 by going through the repeated procedures explained in *Port Nullification*. Then the augmented N_2 become an inactivated network.

The proof of Theorem 3 follows directly from Property 3 and the definition of inactivated networks.

Theorem 3 simply means that, given a network N_2 ran by another network N_1 through m ports $j(V_j, I_j)$, for $j = 1, 2, \dots, m$, there will be no change in the operation of N_2 if the following two operation take place. i) Port j is augmented with voltage and current sources V_j and I_j , for all $j = 1, 2, \dots, m$, and ii) N_1 is depleted of all its sources. This is, in fact, the key issue in conducting a new method of circuit simulation for desired OPs in nonlinear circuits.

Property 5: Any powerless network is an inactive network, but the converse is not necessarily true.

The fact that any powerless network is inactive is evident. For the second part, according to Theorem 3, to inactivate a network its ports must be nullified, and nullification of a port needs augmenting it by sources, as discussed in *Port Nullification*.

Again like nullification, inactivation of a network does not necessarily mean closing its *gates* to the outside world, but it is rather a procedure of conditioning (biasing) the network for a desire operation. In fact, one difference between inactivation of a network and biasing it is that in the former case we move the coordinates to the OP, on the characteristic curve, while in the case of biasing we move the signal to the OP. This means that by inactivation we locally condition the nonlinear devices for linear modeling of the circuit rather than biasing the entire circuit.

Theorem 4:- General-Additivity: Consider an m-port network N_2 connected to another network N_1 that contains several sources. Group the sources in N_1 into n mutually exclusive groups. Then the total effect of network N_1 on N_2 , due to all those sources in N_1 , can be determined by adding n times the effect of N_1 on N_2 , where a) each time a different group of sources is used in N_1 , and b) network N_2 is inactivated before each time the operation is performed.

Theorem 4 is identical to Theorem 2 except that Theorem 2 is for one-port networks, and Theorem 4 is for multiple ports. The proof, therefore, must also be identical with that of Theorem 2. This is true because inactivation, by the definition and Theorem 3, is the same as nullifying all the ports in N_2 .

IV. IMPLEMENTATION AND AN EXAMPLE

The method discussed so far can be implemented on any nonlinear circuit or device. If, however, multiple numbers of nonlinear devices are used in a circuit we can handle the case in two different ways. One method is to take each nonlinear device as a separate entity and deal with it as a nonlinear network. The second method is to group all (or partial) nonlinear devices into one nonlinear network and handle them collectively. Although the later method shows some merit, but because of some complexity involved in the procedure we only consider the former case, i.e., we deal with nonlinear devices individually in this article.

Within the three major semiconductor components, diodes, BJT and MOS, p-n junction diodes are one-port devices and the rest are multiple-port. BJTs are typically two-port devices, but they can be turned into two one-port devices if *Ebers-Moll* large signal models are used [11]. MOS transistors are considered three port device but only four sources are needed for port nullification. For the drain-source port we need to nullify I_D and V_{DS} , for the gate-source we need to nullify V_{GS} , and for the substrate-source we need to nullify V_{BS} to inactivate the entire MOS device.

Due to lack of space we limit our implementation to only one example of a BJT amplifier.

Example 2 – A BJT Feedback Amplifier: For this example we take a two stage npn – pnp amplifier with feedback, as shown in Fig. 8(a). We consider three dc sources for this amplifier, $V_{CC} = 10V$, $V_{EE} = 10V$, and $V_{BB} = 1.1V$. In normal situation the transistors are biased and the input signal v_s will generate the output signals in the amplifier, as depicted in Fig. 8(b). Next, we adopt a supply sequence in three steps as: i) $V_{CC} = 10V$, ii) $V_{EE} = 10V$, and iii) $V_{BB} = 1.1V$, and inactivate the devices, by nullifying the ports, after each step. Table 1

show the supply sequencing applied in this example and the augmented source value in each step of the operation. Obviously, this is only one choice of supply sequencing adopted other grouping and sequencing will end up with the same final result, but possibly with different convergence speed. Figs. 9(a) and (b) show the transistors being inactivated at the last step in the procedure, and Fig. 10(a) indicates the amplifier when it is exhausted of all its dc sources, and the transistors are replaced by the inactivated equivalents. Finally, Fig. 10(b) shows the response of the amplifier to the ac source v_s .

Before we leave this example we need to discuss several important points:

- When we compare the simulated results from the original amplifier, Fig. 8(b), with those from the amplifier with inactivated devices, Fig. 10(b), we notice their differences in dc levels. In Fig. 8(b) both dc and ac signals are present at the outputs, and for the removal of the dc from the output we normally need to use coupling capacitances. While in the case of inactivated devices all node voltages and element currents in the amplifier carry only the ac signal.
- In Table 1 we notice that the last column, representing the sum of all supplies, is the algebraic sum of the other three columns, each representing one of the supplies. This is the *additivity* property, stated in Theorem 4.

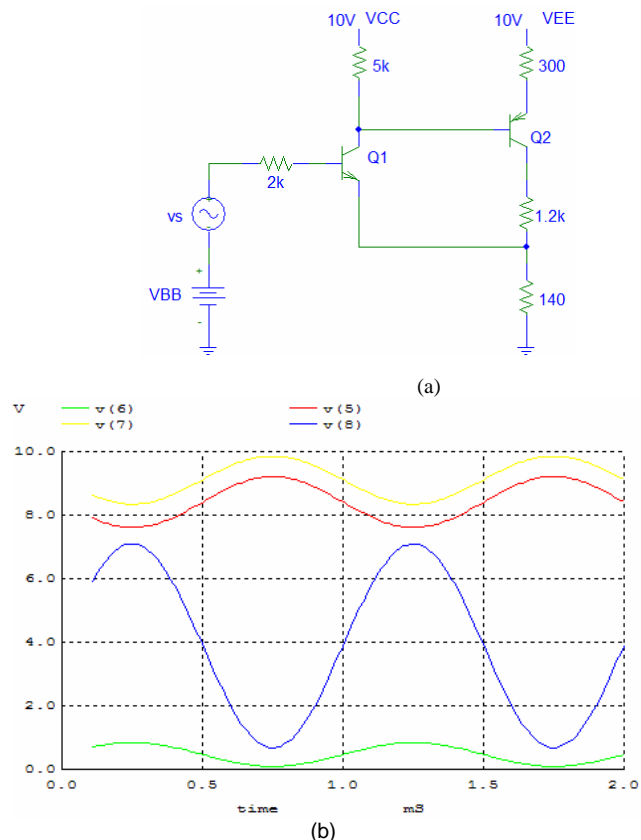


Fig. 8(a) - A two stage feedback amplifier, (b) The output responses

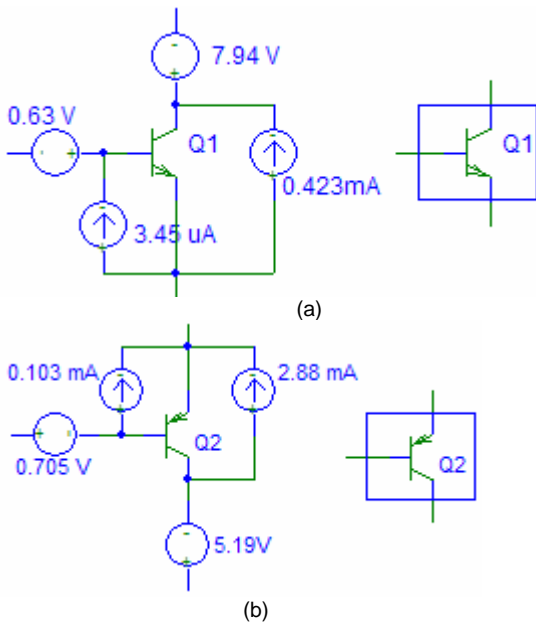


Fig. 9 – Inactivation of the BJTs, (a) the npn, and (b) The pnp

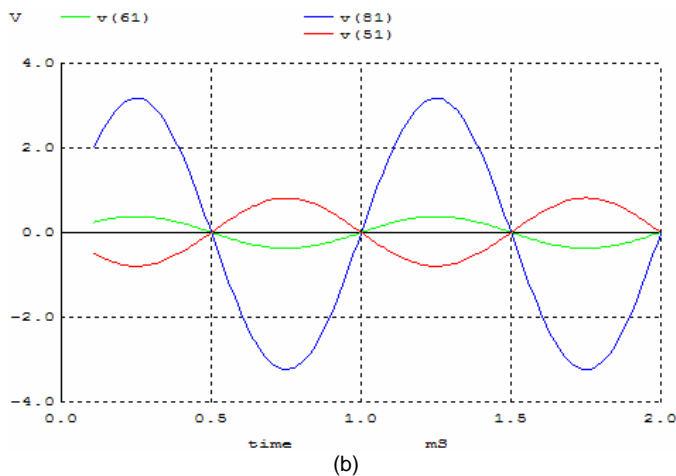
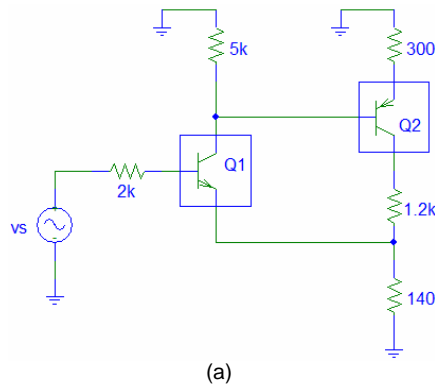


Fig. 10(a) - The feedback amplifier after the devices' inactivation, and (b) the output responses

TABLE I
THE BJTs INACTIVATION RESULTS IN SUPPLY SEQUENCING

Sequence of Sources	V _{CC}	V _{EE}	V _{BB}	All Sources
V _{BE1}	-1.23e-08	-1.54e-09	6.30e-01	6.30e-01
V _{CE1}	1.00e+01	3.87e-09	-2.06e+00	7.94e+00
I _{B1}	1.64e-12	-5.49e-19	-3.45e-06	-3.45e-06
I _{C1}	-1.30e-11	1.78e-15	-4.23e-04	-4.23e-04
V _{EB2}	-1.00e+01	1.00e+01	7.05e-01	7.05e-01
V _{EC2}	-1.35e-07	1.00e+01	-4.81e+00	5.19e+00
I _{B2}	1.01e-10	-1.08e-12	-1.03e-04	-1.03e-04
I _{C2}	-1.00e-10	-1.10e-11	-2.88e-03	-2.88e-03

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