

Local Biasing and the Use of Nullator-Norator Pairs in Analog Circuits Designs

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Abstract—Although local biasing of components used in an analog circuit is shown to be a very attractive design methodology, significantly simplifying the design procedure [3], it makes the DC supplies distributed and often not in desired locations in the circuit. In response to this problem a new technique is developed that in conjunction with the local biasing it handles the DC supply sources very smoothly and transfers them to the designated locations in the circuit, specified for global biasing. The technique utilizes nullator-norator pairs to do the required source transformation. Overall, the technique totally avoids nonlinearity in the operation due to a novel nullator modeling that is presented for locally biased components. For the lack of space, the method is only applied to MOS transistors here, but it can simply be extended to BJTs as well. As an example, a two stage amplifier with feedback is used to demonstrate the methodology.

Index Terms—Analog Circuit Design, Local Biasing, Nullator-Norator Pairs, and Source Transformation.

I. INTRODUCTION

FINDING the right operating points is a great challenge in analog designs. It becomes more complex as the number of nonlinear components in the circuit increase and the design requirements become tighter and more efficient designs are asked for. The biasing problems are mainly two; one deals with nonlinearity of the circuit that results from nonlinear components. The second problem is the lack of separability between the linear and nonlinear components. In general, no method exists to locally treat the hard nonlinearities in the circuit. Recently a method using local biasing of nonlinear components in analog circuits has been introduced [3] that deals with both specified problems. By local biasing the nonlinear components are DC-isolated from the circuit, while they operate normally at their designated operating points for AC signals. However, the problem with the local biasing is that the supply (current and voltage) sources that are used to locally bias the components may not end up being in the right locations in the circuit. In addition, accommodating multiple supplies in a circuit creates practical problems, although current mirroring and using voltage dividers may help to make it tolerable.

In the proposed method we follow two steps for DC biasing of analog circuits. In the first step we go through a local biasing technique and bias the individual components within the circuit. In the second step, we try to replace the local biasing sources with limited number of circuit supplies

assigned to designated locations. In this method, we use nullor pairs as a mean to transfer the distributed sources used for local biasing to locations that are pre-assigned for the global biasing of the circuit.

The use of nullor pairs is not, of course, new in analog circuit design [1,2]. Claudio Beccari [1] uses the nullator-norator pair eloquently to find and allocate the transmission zeros in a circuit. Telelo-Cuautle also introduces a biasing technique that utilizes nullor pairs [2]. However, the method proposed in this article is using the nullor pair differently for DC biasing. First, it applies local biasing to the nonlinear components in the circuit. By doing so, it establishes the entire biasing of the circuit for the desirable operating regions. In the second step the method replaces the pre-biased components and their biasing sources with linear models that contain nullators. Next, the nullators are paired with norators that are actually the place holders of the global and final biasing (current or voltage) supplies.

II. LOCAL BIASING

First we need to define some terms that are used in this article [3]. Also, all our discussions here apply to DC biasing, unless stated otherwise.

Null Port: Consider two networks N_1 and N_2 connected through a port $k(v_k, i_k)$. Port $k(v_k, i_k)$ is said to be null if both voltage v_k and current i_k are zero.

Port nullification: Consider two networks N_1 and N_2 connected through a port $j(v_j, i_j)$. Port $j(v_j, i_j)$ is nullified if it is augmented, from both sides (N_1 and N_2), by current sources i_j and voltage sources v_j so that a null port $k(v_k, i_k)$ is created as a result, as shown in Fig. 1.

Apparently, there will be no change in the currents and voltages within both networks N_1 and N_2 if we disjoint them at port $k(v_k, i_k)$ and connect each to a nullator, as shown in Fig. 2. This results in a new finding as follows.

Dsource: A two terminal element in a circuit is called a Double-source, or Dsource, if both voltage across the

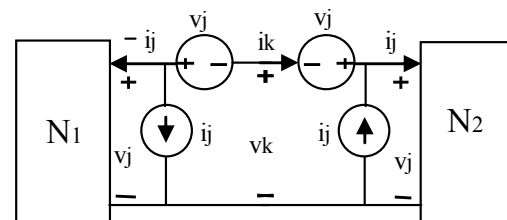


Fig. 1 - Port nullification procedure

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terminals and the current through the element represent two

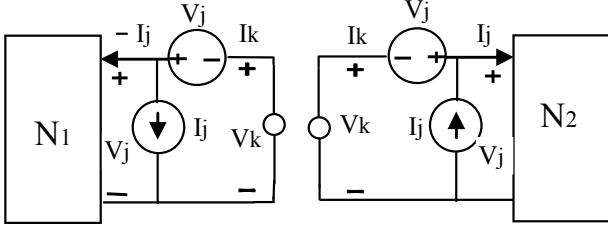


Fig. 2 - Two networks N_1 and N_2 disjointed at port $k(v_k, i_k)$ and each terminated by a nullator.

independent sources.

One way to create a Dsource with voltage V and current I is to have a nullator parallel with a current source I and in series with a voltage source V , as depicted in Figs. 3(a) and (b). Also notice the difference between the two Dsources $Ds(V, I)$ and $Ds(I, V)$ in the figure. In $Ds(V, I)$ the voltage source V provides (or consumes) power and the current source I is sitting idle; while in $Ds(I, V)$ the current source I provides (or consumes) power and the voltage source V is sitting idle.

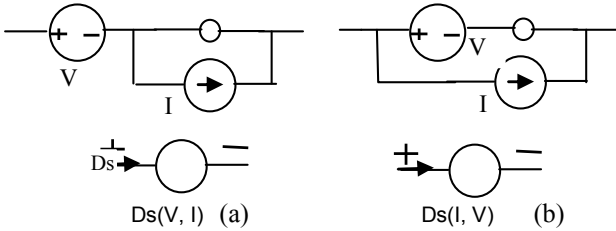


Fig.3 – Dsources and their symbols; (a) voltage Dsource; (b) current Dsource

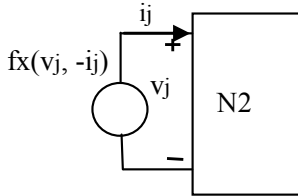


Fig. 4 – Network N_2 terminated with a Dsource

N_2 are terminated with two Dsources. This leads to the following property.

Property 1: Consider two networks N_1 and N_2 connected through a port $j(v_j, i_j)$. There will be no (current or voltage) change in network N_2 if N_1 is removed and is replaced with a Dsource $Ds(v_j, -i_j)$, as shown in Fig. 4.

Now we turn into defining local biasing.

Local biasing (LB): A port is locally biased if it is nullified. Likewise, a network or a component is locally biased if all its ports are nullified.

Apparently, local biasing of a network or a component is not unique. A port can be locally biased for any selection of an operating point on its characteristic curve. This is also true for a component with multiple ports. Evidently, connecting a locally biased device to a network with no DC (voltage or current) supply does not change the biasing condition of the device. This simply means that a locally biased device does not need any external DC supply to keep it operating.

Note that when we locally bias the nonlinear components within a circuit, we in fact replace the DC power supplies in the circuit with local sources that are only responsible to provide biasing/power to the individual devices. This certainly

gives a choice to the circuit designer to select his/her own operating regions for the nonlinear devices without going into iterations, typically required for nonlinear designs [4]. Second, local biasing allows the designer to locally tune the circuit and make changes without disturbing the other parts of the circuit. Third, it is shown that local biasing minimizes the DC power consumption in the circuit [5]. As the result, it is being shown that in a locally biased situation the (voltage and current) signals are always AC except in the nonlinear devices that are locally biased both AC and DC are present.

Within the three major semiconductor components p-n junction diodes are one-port devices. Bipolar-junction transistors are generally considered two-ports, but they can be turned into two one-port devices if Ebers-Moll large signal model is used. MOS transistors are considered three-port devices but only four sources are used to locally bias the device. This is because for the drain-source we need both I_D and V_{DS} sources to nullify the port, where as for the gate-source and the substrate-source we only need V_{GS} and V_{BS} to nullify the ports, respectively. Figure 5 shows an NMOS and a PMOS being locally biased with their symbolic representations also shown. However, for simplicity we are going to drop the substrate effect, V_{BS} , later in our discussion.

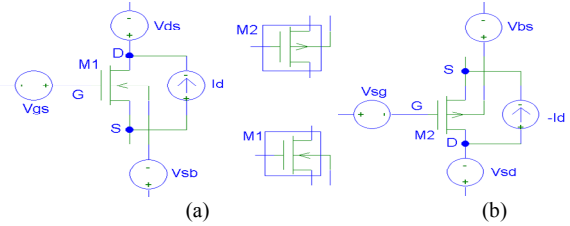


Fig. 5 - Locally biased (a) NMOS and (b) PMOS Transistors with their symbolic representations

III. GLOBAL BIASING

With all advantages of the local biasing, one major disadvantage still remains and that is “supply distribution” through out the circuit. Although by mirroring current sources and also by providing power through voltage dividers the problem may be reduced; but over all, this makes the design vulnerable, costly and almost impractical. Obviously, we cannot have both worlds without compromising. The question is whether it is possible to preserve the traditional biasing (global biasing) and also keep the advantages of local biasing at the same time? The answer is affirmative, as we can see. For faster and better design procedure we definitely need to start from local biasing. This is mainly because it linearizes the circuit design. Second, it separates parts of the circuit and deals with them independently. Again, the difficulty is the existence of numerous DC sources being used through out the circuit which we definitely need to find ways to transfer them to the locations designated for global biasing.

To deal with the problem we first need to introduce one of the critical links bridging between local biasing and global biasing, which is nullator, particularly in Dsource structure. We start with the following important properties.

Property 2: A locally biased component within a network N can be removed and be replaced with nullators, one for each

port, without affecting the currents and voltages within the network N .

Again, note that locally biasing a component produces zero voltages and zero currents at its ports without affecting its internal currents and voltages. This simply means that, in an analog circuit when certain components are locally biased they can be separated and removed from the main circuit without imposing any effect on the circuit operation or on the biasing conditions of those components themselves, provided that each disjointed port, from both sides, is connected to a nullator.

Property 3: A two terminal component in a circuit, such as a p-n junction diode, that is biased by current I_D and exhibits a junction voltage V_D can be replaced with a Dsource $Ds(I_D, V_D)$ without causing any change in the currents and voltages within the rest of the circuit.

Property 3 directly results from Property 1. Note that $Ds(I_D, V_D)$ models a diode only when the diode is in a circuit and biased with I_D and V_D . Property 3 can also be extended to include the components with multiple ports such as bipolar and MOS transistors. Figure 6 shows the Dsource models of nMOS and pMOS transistors when they are (globally) biased for V_{GS} (V_{SG}), V_{DS} (V_{SD}), I_D , and V_{BS} (V_{SB}).

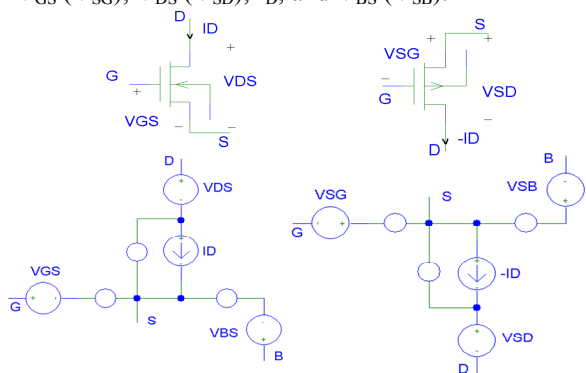


Fig. 6 - Dsource models of nMOS and pMOS transistors when globally biased for V_{GS} (V_{SG}), V_{DS} (V_{SD}), I_D , and V_{BS} (V_{SB}).

It is interesting to see the relationship between a locally biased MOS transistor (as indicated in Fig. 5) and its Dsource model, as shown in Fig. 6. If we simply replace each nullator in Fig. 6 by its equivalent locally biased port (from Fig. 5) and then perform source cancellations, we will end up with MOS transistor alone that has no augmented source attached; but the difference is that the transistor is (globally) biased with pre-specified V_{GS} (V_{SG}), V_{DS} (V_{SD}), I_D , and V_{BS} (V_{SB}). This basically means that, when we replace each transistor with its Dsource model we have in fact removed the local biasing source but have left the transistor desirably (globally) biased. At this point all we need to do is to employ power supplies that are needed to provide this global biasing to the components. To address this problem we need to do the following.

The methodology of assigning power supplies for the (global) biasing can be carried out in two steps. In the first step we designate locations in the circuit for the DC power supplies (both voltage and current sources) but with values still unspecified. Evidently, each of these power supplies can be represented by a norator. Therefore, the circuit so far

obtained is going to be a linear circuit that containing nullator-norator pairs (provided that the number of nullators and norators match). In the second step we need to solve the circuit equations and get the DC supplies (norators) evaluated.

IV. IMPLEMENTATION AND AN EXAMPLE

In the previous section, we noticed that to move from local biasing to global biasing Dsource models of the transistors will help and totally linearize the design procedure. We can state the problem as follows: Given the topology of an analog circuit to be designed with specified components and specified regions of operations for its transistors (or any other nonlinear components) find the value of the DC supplies (voltages and currents) in the designated locations so that the design criteria are met. Based on the methodology introduced in Section III and to perform the design in steps we propose Algorithm 1. Without loss of generality we present the algorithm only for MOS circuits here.

Algorithm 1:

1. Replace each MOS transistor with its Dsource model as indicated in Fig. 6. In this modeling the values of V_{GS} (V_{SG}), V_{DS} (V_{SD}), I_D , and V_{BS} (V_{SB}) are those specified by the designer or the design criteria
2. Identify the locations of the DC supply (voltage and current) sources in the circuit and replace the unknown DC sources by norators. Note that the number of norators must match with the number of the nullators present in the Dsource models to produce nullor pairs.
3. Now, we are facing with a totally linear circuit with the presence of the nullor pairs. Solution to this circuit problem provides values for the norators in the circuit, which are indeed the DC supplies for the design. Notice that both voltages and currents of each norator will be found and it is up to the designer's choice to assign a voltage supply or a current supply to the location.

Now that we are done with the (DC biasing) design there are still some issues that must be dealt with before we leave the subject. First, as mentioned earlier, the equivalency of number of nullators and norators is necessary to solve the circuit equations and find the norator values but this is not sufficient. In a way, the problem is related to the independency in the circuit (KCL and KVL) equations, where no loop of voltage sources and no cutset of current source are allowed. There are of course more details to be discussed in this regard which we drop here because of the lack of space. The second problem is the fact that with each transistor added to the circuit at least two (if we ignore the substrate effect) nullators are added to the linear circuit; whereas the number of supplies (including the current mirrors and voltage dividers) are usually much more limited. To handle this problem, we need to prioritize the design specs so that the most critical criteria come first and we stop when the numbers match the number of supplies.

The following example demonstrates the design of a two stage MOS amplifier with feedback using Algorithm 1.

Example: Consider a two stage MOS amplifier with feedback [6], shown in Fig. 7. The schematic provides only

the topology of the design and the circuit values are left to be specified. We start the design by first selecting values for V_{GS} (V_{SG}), V_{DS} (V_{SD}), and I_D for the two MOS transistors as given in Table 1 (for simplicity the body effect is ignored). Next, the selected DC voltages and currents are incorporated into the Dsource models of the transistors (Fig. 6). These models are then substituted for the transistors in the circuit. According to Algorithm 1, the next step in the design is to identify the locations of the DC supplies for the global biasing, namely V_{DD} , V_{SS} , V_{GG} , and I_S . Hence, we assign one norator for each unspecified supply and form a linear circuit for the design with nullor pairs, as depicted in Fig. 8. Note that the number of norators and nullators match in this circuit.

TABLE 1 – INITIAL OTA LINEAR MODEL SPECIFICATIONS

Device	V_{GS}	I_D	V_{DS}
M1	2.0 V	140 μ A	1.8 V
M2	-1.7 V	-120 μ A	-2.6 V

We are now ready to solve the linear circuit with nullor pairs. SPICE cannot directly solve the circuit equations with nullor pairs; but if we replace each pair carefully with an ideal OP-Amp the simulator will provide the entire currents and voltages within the circuit, including the voltages or currents for the norators. Now it is our choice to replace each norator with a voltage source or a current source. Other circuit parameters such as resistor values can also be assigned, or at least adjusted, at this stage of the design. One advantage of this assignment is that if the DC voltage supplies, resulted from the analysis, are not within the conventional rating we might be able to make correcting adjustments by using right resistor values (details are postponed for another publication). Another point of caution is that, this Dsource modeling of transistors is developed for DC biasing. For AC analysis and design of analog circuits we still need to replace the transistors with their linear small signal models. The advantage of Dsource modeling, however, is its direct reference to the specified operating points for each device; hence, to find the linear model of the device we only need to refer to the device characteristics at those operating points.

For the present and after making several resistor value adjustments we find: $V_{DD} = 5V$, $V_{GG} = 3.1V$, $V_{SS} = 5V$, and $I_D = 60 \mu A$; and the resistor values are adjusted to: $R_1 = 11K$, $R_2 = 45K$, $R_3 = 15K$, $R_4 = 3.3K$, and $R_5 = 20K$. This completes the DC biasing of the feedback amplifier as being configured in Fig. 7. Finally, the MOS transistors are sized to deliver the design criteria as: $L = 2 \mu m$, $W_n = 20 \mu m$ and $W_p = 60 \mu m$. Finally, Table 2 shows the SPICE simulation results for the design, and compared to Table 1 we are within 5% accuracy.

TABLE 1 – THE OTA RESPONSE USING SPICE SIMULATION

Device	V_{GS}	I_D	V_{DS}
M1	1.95 V	137 μ A	1.9 V
M2	-1.7 V	-118 μ A	-2.66 V

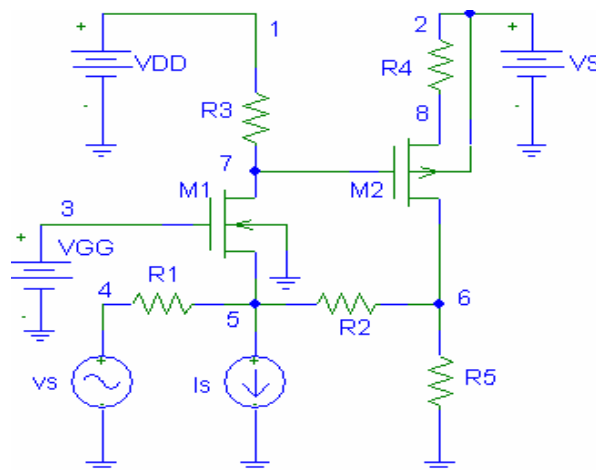


Fig. 7 – Initial configuration of a MOS feedback amplifier

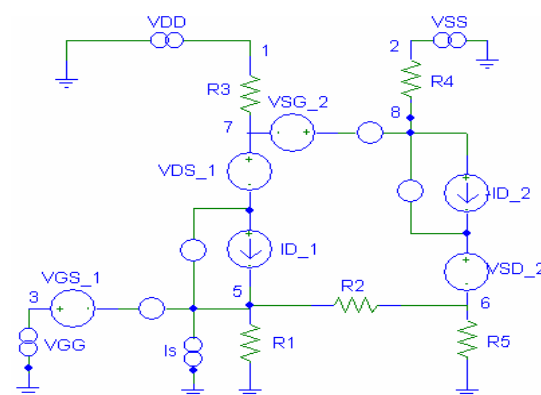


Fig. 8 – The linear DC modeling of the amplifier using fixorce modeling concept for the MOS transistors

CONCLUSION

A new approach to design of analog integrated circuits is presented. Through local biasing we have been able to achieve the desired performance for the circuit we like to design. The technique is based on designing the core with only sources that are used to locally bias the transistors. Later these sources are transferred to appropriate locations in the core by using nullator pairs. This linearizes the circuit and leads to a new circuit topology that makes it possible to replace the local biasing sources with final current mirrors and power supplies.

REFERENCES

- [1] Claudio Beccari "Transmission zeros", Dipartimento di Elettronica, Turin Institute of Technology, Turino, Italy; December 6, 2001.
- [2] E. Teleo-Cuautle, L.A. Sarmiento-Reyes, "Biasing analog circuits using the nullor concept", Southwest Symp. on Mixed-Signal Design, 2000.
- [3] R. Hashemian, "A Methodology to Simulate Circuits with Nonlinear Devices," Proc. of MWSCAS 2005, Cincinnati, Ohio, August 7, 2005.
- [4] ____, "New Analysis and Design Technique for Analog Circuits ", Proceedings of the 2006 IEEE International Midwest Symposium On Circuits And Sys., San Juan, Puerto Rico, August 6 – 9, 2006.
- [5] ____, "Analog Circuit Design with Linearized DC Biasing ", Proceedings of the 2006 IEEE International Conf. on Electro/Information Technology, Michigan State University; Lansing, MI, May 7– 10, 2006.
- [6] R. Jacob. Baker, "CMOS, Circuit Design, Layout, and Simulation," 2nd ed. Wiley Interscience, 2008, pp. 613 – 823.