

# FPGA e-Lab, a Technique to Remote Access a Laboratory to Design and Test

Reza Hashemian, Life Member IEEE  
Northern Illinois University,  
[reza@ceet.niu.edu](mailto:reza@ceet.niu.edu)

Jason Riddley  
Northern Illinois University,  
[jrriddley@gmail.com](mailto:jrriddley@gmail.com)

## Abstract

*We are proposing a new remote access system that allows for laboratory experiments to be performed remotely in the classroom or anywhere an internet terminal is available. The system specifically employed is aimed at courses of digital design using FPGA platforms. It is a powerful tool that allows for instruction with experiments and design examples in the classroom and gives students full access to laboratory equipment and an FPGA platform remotely from an internet terminal. This system is called FPGA e-Lab. It is constructed of a Xilinx Spartan-3E Starter Kit whose hardware is interfaced through a laboratory PC via an interactive LabView Graphical User Interface (GUI) and acquisition hardware as well as RS-232 serial and USB ports. Microsoft XP Remote Desktop is the vehicle used to access the Lab PC from a remote location.*

## 1. The Proposed Methodology

The objective of this presentation is to introduce the FPGA e-Lab system in both its construction and its importance to engineering education. The system will open up traditional laboratory courses to students who have a need for internet based instruction. For students who have physical access to the laboratory equipment, the experimentation experience can be enriched by allowing more time for the students to work beyond “lab hours” either for assignments or curiosity. The e-Lab can also be used to enhance the learning experience in the classroom with experiments complimentary to instruction making for more interesting and fun lectures without the need or confusion of bringing the lab into the classroom. The e-Lab could also be used to bring education institutions together for collaboration. This could be to put together funds to purchase more advanced equipment that any institution by itself could afford and then to be shared via the e-Lab. Or, the collaboration could be to outreach to disadvantaged institutions whose students would not normally have access to quality lab equipment.

The FPGA e-Lab system is composed of hardware and a “Laboratory Protocol” so that the system can be used and be used effectively by students. To orchestrate effective use of the system, we will first describe the stages of the digital design process or design flow for student experiments. For FPGA designs, the flow as is follows:

1. Project description and specification.
2. Design entry through schematic capture and/or Hardware Description Languages such as VHDL or Verilog.
3. Functional simulation and design verification.
4. Design synthesis.
5. Design implementation, and post place and route simulation.
6. FPGA hardware reconfiguration.
7. Design verification: testing and debugging.

As for the second step, we grouped these stages based upon what software or hardware tools needed for each stage of the design and came up with laboratory rules and regulations in order to minimize problems such as lab congestion. Stages 1 through 5 do not require hardware access but only software tools that are freely available for download online from Xilinx and other vendors. Therefore, the students will be required to complete these stages outside and before entering the FPGA e-Lab environment although the tools are available for making modifications. For stages 6 and 7, students will access the FPGA e-Lab environment to program the FPGA development board, experimentally verify their designs, and make modifications, resynthesize, and retest if needed. Finally, step three is currently undergoing development and will involve other departments and expertise and involves implementing the rules and regulations for students to use the system. These regulations would include student eligibility, access periods, and student schedules. The goal is to make access convenient for those who are only able to get to a computer terminal at certain times even when lab equipment is limited and congestion is heavy, such as during finals or before projects are due.

