

# Use of Local Biasing in Designing Analog Integrated Circuits

Reza Hashemian<sup>1</sup>, *Life Member, IEEE*

**Abstract**—A new biasing technique called “local biasing” of transistors is used to design analog integrated circuit amplifiers, or any other analog ICs. The technique is based on designing the circuit without any external source but only the sources that are used to locally bias the transistors [12, 13]. Later these sources are transferred to appropriate locations in the circuit which leads the circuit to a new topology and configuration that makes it possible to replace the local biasing sources with final current mirrors and one or two conventional power supplies. Local biasing is revisited, and an OTA design example is provided to clarify the methodology and demonstrate the procedure.

**Index Terms**—Analog circuit Design, Integrated Circuits, Local Biasing, and Source Transformation.

## I. INTRODUCTION

THE major dealing with nonlinear circuits is the biasing for the right operating regions; i.e. getting desirable operating points with fast convergence [1 – 8]. The problem is that the biasing gets harder as the analog circuits advance and get more complex. The analysis of such circuits may even lead to multiple DC operating points [9], or causing instability because of the existence of positive feedbacks in the circuit [9, 10, 16].

There are numerous causes for these problems. One difficulty stems from the fact that in the traditional method an analog circuit is usually analyzed and simulated as whole – linear and nonlinear components all together. This certainly makes a quick and smooth convergence difficult for large circuits. In addition a poor selection of the initial conditions plus large and unregulated steps of iterations can cause the circuit to diverge. An additional difficulty may result from a fixed circuit configuration. For instance, applying DC supplies to certain pre-assigned locations in the circuit may not always be the best choice, and floating the supplies first may result in a better biasing and quicker convergence in certain design situations; and for directing the supplies to their final destinations in the circuit, after the analysis is done, we can always use methods such as source transformation to move them around. Another problem with the global biasing is that it cannot address local changes and modifications without actually going through the entire circuit. For example, if some operating points do not meet the design criteria or a few components are replaced during the design the circuit needs to

go through the entire biasing process again.

In a recent development [11, 15] a new methodology is introduced that helps to separate nonlinear devices from the linear portion in a circuit. The nonlinear devices are individually biased to operate at their desirable regions; and the entire circuit is then put together without any extra DC power supply added to the circuit. The method is proved to be smooth and highly controllable; and it follows an additivity property [13] that has been only possible for linear circuits. In case of the design, the method makes it to avoid any nonlinear behavior of the circuit, and directly address the performance and the criteria of the design. Finally, because the new development offers a complete isolation of individual nonlinear devices, it makes it possible to locally modify, adjust and tune the circuit without disturbing the rest of the circuit. This feature is interesting and useful for designs that need partial modifications, such as replacing the transistors in an amplifier with different types.

However, the major problem in this methodology is the possibility of abundant number of supplies (DC voltage and current sources) and unconventional locations that they usually occupy. One way to deal with this problem is to use source transformation [1, 2] to bring all sources together and possibly replace them with one or two conventional supplies such as  $V_{DD}$  and  $V_{SS}$ .

What is presented in this article is to use local biasing to design analog integrated circuits; and to smoothly move from local biasing to global biasing. For this we first employ local biasing to design a generic analog circuit; next we will try to reallocate the local biasing supplies in an arrangement that it becomes possible to combine the sources and reduce them to only a few, for all practical purposes. The current sourcing and mirroring, typically employed in analog integrated circuit designs, are strong tools [17] and dominantly used here to get the source distribution for the final circuit configuration.

The rest of the materials are arranged as follows. Section II of the paper introduces the local biasing of circuit components. Local biasing of NMOS and PMOS transistors are discussed in Section III. An algorithm is also developed in this section that is used to implement the local biasing for analog IC design. An example is worked out in Section IV that shows the implementation of the local biasing in designing an OTA circuit. Finally we conclude our discussion in Section V.

<sup>1</sup> Reza Hashemian is with Northern Illinois University, Dept of Electrical Engineering, DeKalb, IL; phone: 815-753-9930; fax: 815-753-1289; e-mail: reza@ceet.niu.edu.

## II. LOCAL BIASING

First we need to define some terms that are used in this article [14]. Also, all our discussions here apply to DC biasing, unless stated otherwise.

**Null Port:** Consider two networks  $N_1$  and  $N_2$  connected through one or more ports. A port  $j(v_j, i_j)$ , common between  $N_1$  and  $N_2$ , is said to be null if both the current through the port,  $i_j$ , and the voltage across the port,  $v_j$ , are zero. This apparently is nothing to do with the values of the currents and voltages in other ports or even the currents and voltages in  $N_1$  or  $N_2$ .

**Port nullification:** Consider two networks  $N_1$  and  $N_2$  that are connected through one or more ports. A port  $j(v_j, i_j)$ , connecting  $N_1$  to  $N_2$ , is nullified if it is augmented, from both sides ( $N_1$  and  $N_2$ ), by current sources  $i_j$  and voltage sources  $v_j$  so that a null port  $k(v_k, i_k)$  is created as a result [14], as shown in Fig. 1.

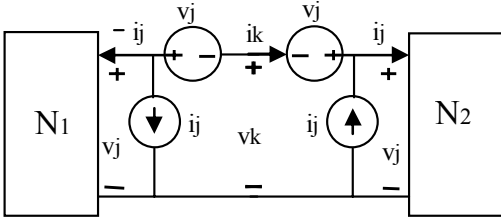


Fig. 1. Port nullification procedure

**Local biasing (LB):** A port is called *locally biased* if it is nullified. Likewise, a network or a component is locally biased if all the ports in the network or component are nullified. Again, note that a locally biased component exhibit zero voltages and currents only at its ports; otherwise its internal currents and voltages are unaffected. Also note that local biasing of a port or a device is not unique. A port can be locally biased for any selected operating point on its characteristic curve. This is also true for a device.

It becomes evident now that connecting a locally biased device to a network that has no DC supply does not change the biasing condition of the device. This simply means that, a locally biased device does not need any external DC supply to keep its biasing (operating region).

## III. LOCAL BIASING OF TRANSISTORS

The technique discussed so far can be implemented on any nonlinear circuit or device. If multiple numbers of nonlinear devices are used in a circuit we can handle the case in two different methods. One method is to take each nonlinear device as a separate entity and deal with its ports as a nonlinear network connected to the rest of the circuit. The second method is to group all (or part of) nonlinear devices into one nonlinear network and handle them collectively. Here we only consider the former case, i.e., dealing with nonlinear devices individually.

Within the three major semiconductor components p-n junction diodes are one-port devices; hence, one-port

nullification biases a diode. Bipolar-junction transistors are generally considered as two-port devices, but they can also be treated as two one-port devices if Ebers-Moll large signal is used to model a transistor [11]. MOS transistors are considered three-port devices (gate-source, drain-source, and substrate-source) but only four sources are needed to locally bias the device. This is because the drain-source port is the only one that needs both  $I_D$  and  $V_{DS}$  sources to nullify the port. For the gate-source and the substrate-source we only need to use  $V_{GS}$ , and  $V_{BS}$  sources, respectively, to nullify the ports. Figure 2 shows an NMOS and a PMOS locally biased with their symbolic representation shown. However, for simplicity reason we are going to drop the effect of substrate-source,  $V_{BS}$ , from our discussion.

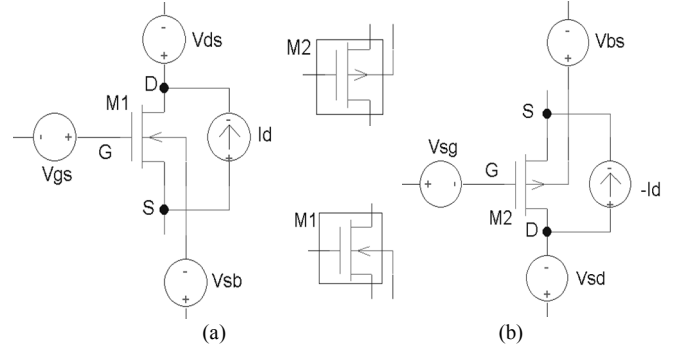


Fig. 2. Locally biased (a) NMOS and (b) PMOS Transistors with their symbolic representations

For bipolar transistor Fig. 2(c) shows a locally biased npn transistor with its symbolic representation.

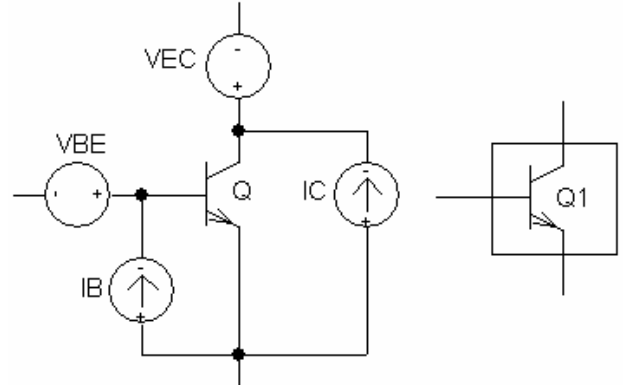


Fig. 2(c) – Locally biased BJT with its representation.

Figure 3 shows a locally biased NMOS diode along with its equivalent linear model also biased, where  $r_{ds} = V_{ds}/I_d$ . This is particularly useful in designing current sources and current mirrors. Similarly, Fig. 4 (a) shows a resistance  $R$  locally biased for current  $I_R$ . Note the similarity between the MOS diode model and the resistance when they are both locally biased.

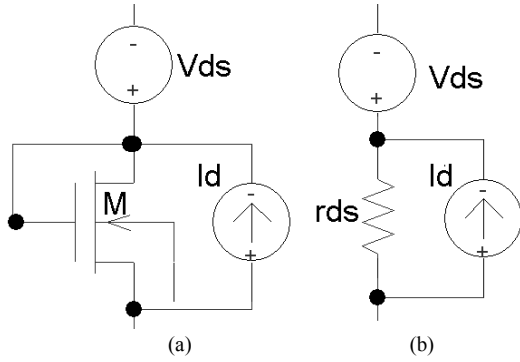


Fig. 3. (a) An NMOS diode with locally biased for  $I_d$ ; and (b) the equivalent linear model of the diode after being locally biased.

It is also important to note, from Fig. 4, that for  $V_R = R * I_R$  both components in (a) and (b) represent the same resistance  $R$  with identical terminal characteristics, except in (a)  $R$  is biased with current  $I_R$  while it is not in (b). Evidently, this identity is the result of super position which is only valid for linear components, such as resistances, and not necessarily valid for nonlinear components such as transistors.

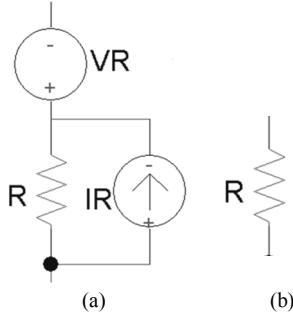


Fig. 4. a) A resistance  $R$  after being locally biased for current  $I_R$ ; b) an unbiased resistor  $R$ .

Algorithm 1 presents a step-wise procedure for the design of an analog integrated circuit with specified criteria and performances.

#### Algorithm 1:

Given an analog circuit specification and the performance criteria needed we first assume certain topology for the initial design with major (transistor) drivers being specified.

1. Based on the circuit specifications we can always assume certain operating regions for the transistors so that the drivers can operate to provide the best performance for the design. Next, we locally bias all (linear and nonlinear) components in the circuit, as discussed earlier, and remove the external supplies instead
2. Next we start the process of integration and try to replace the resistances (while locally biased) with their transistor counter parts. This is, of course, a very crucial process in which transistors, or combined transistor components, with similar property must be substituted for the resistive elements in the circuit so that the new components do not undermine the overall

circuit criteria and do not add to the complexity of the circuit.

3. Now, our next job is to combine and transfer the local biasing (voltage and current) sources to the right locations in the circuit so that the ultimate result is the removal of the local biasing sources in favor of one or two power supplies in the circuit and with some additional current sources and current mirrors, if needed.
4. This concludes the design of an analog circuit in integrated circuit configuration.

As we notice from Algorithm 1, there is no dealing with nonlinearity and possible iterations during the entire stages of the design; and this we certainly owe to the local biasing of the nonlinear components.

#### IV. IMPLEMENTATION AND AN EXAMPLE

As an example we consider designing an Operational Transconductance Amplifier (OTA) [17] with some specified circuit criteria. In using the design Algorithm 1, we initially start from a discrete differential pair and a buffer stage, as the core of our circuit, shown in Fig. 5. Table 1 shows the initial design parameter for this generic OTA.

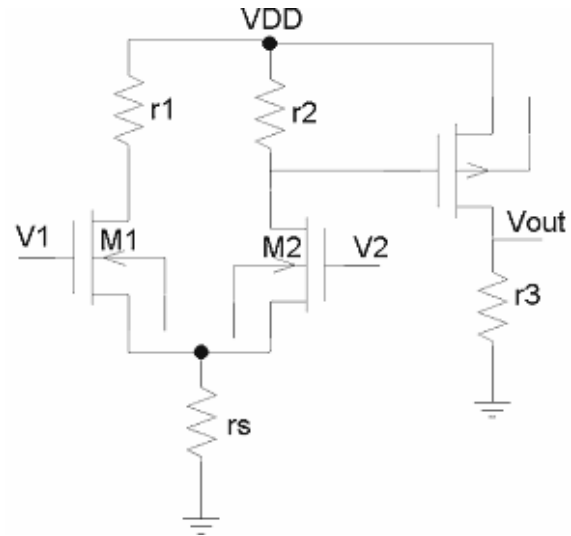


Fig. 5. A preliminary sketch of an OTA differential pair and a buffer stage.

TABLE 1 – INITIAL OTA LINEAR MODEL SPECIFICATIONS

| Param | $I_s$     | $I_{out}$ | $r_s$        | $r_1$       | $r_2$       | $r_3$         |
|-------|-----------|-----------|--------------|-------------|-------------|---------------|
| Value | $20\mu A$ | $10\mu A$ | $50 K\Omega$ | $5 K\Omega$ | $5 K\Omega$ | $150 K\Omega$ |

As specified  $r_1$  and  $r_2$  must be low for OTA but  $r_3$  is relatively high for voltage gain and capacitive load. In addition, to reduce the effect of common mode in the OTA the common mode input impedance must be high; hence  $r_s$  is selected relatively high. Next we are going to preserve the

overall configuration of the OTA and its criteria but replace the linear models with actual transistors in order to make it fully integrated. For this particular example we consider short channel devices with 50 nm process [17]; and for integration we go through the following steps as described in Algorithm 1:

- We begin our design strategy by first specifying the desirable operating points for the OTA components; and this must be done so that the circuit criteria are met.
- Next, we leave out the supply  $V_{DD}$  and instead locally bias all the components (linear and nonlinear) in the circuit so that each component operates at its designated operating region. Figure 6 depicts the new circuit configuration after the components are locally biased (see Figs. 1, 2 and 3). Notice that for this design our target specs are  $I_{d1} = I_{d2} = I_{d3} = 10 \mu\text{A}$ . We also note in Fig. 6 that  $V_{d1} = V_{ds1} + V_{r1}$ ,  $V_{d2} = V_{ds2} + V_{r2}$ , and  $V_{d3} = V_{ds3} + V_{r3}$ , where,  $V_{dsi}$  and  $V_{ri}$  (for  $i = 1, 2,$  and  $3$ ) represent the biasing voltages of the MOS and the resistance in series in each branch, respectively.

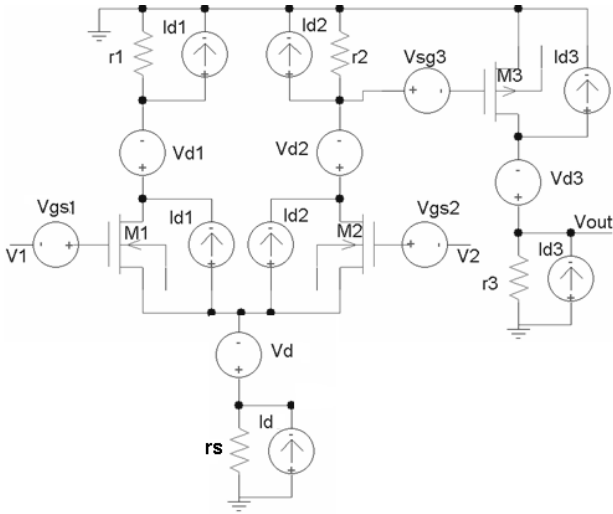


Fig. 6. The preliminary OTA locally biased for a desirable operation.

- Our next step is to move toward the integration and replace the resistors with MOS transistors. As indicated earlier and from the OTA specification [17] the load resistances  $r_1$  and  $r_2$  are low and can be replaced with MOS diodes. Note also the similarity between a resistance and a linear model of an MOS diode when they are locally biased (Figs. 2 and 3). Thus both  $r_1$  and  $r_2$  are replaced with PMOS diode circuits. There is, however, one noticeable difference in this exchange: the biasing voltage sources for  $r_1$  and  $r_2$  is 50 mV, but when they get replaced with the PMOS diodes the source value increases to  $V_{d1} = V_{d2} = 350 \text{ mV}$ . In case of the load resistance  $r_3$ , because of higher impedance situation here, the resistance is replaced with an NMOS current mirror; and in this replacement the biasing voltage source is changed from  $V_{r3} = 1.5 \text{ V}$  to  $V_{d3} = 350 \text{ mV}$ . Finally, the base resistance

$r_s$  is also replaced with an NMOS current mirror. Here again the biasing voltage source  $V_d$  is changed from 1.0 V to 120 mV.

- Applying some simplification results in moving all the voltage sources in each branch to the top, and then combining them and to get them all covered by one or more power supplies. In case of a skillful design, however, it is expected that all the branch voltage sources, after being combined, become identical and therefore could be represented by only one supply  $V_{DD}$ .
- Next it remains to deal with the current sources. We notice that the current sources flowing along each branch (bottom to top) are identical and can be combined into one for each branch. This indicates that we only need three current sources for the circuit to replace them all; and in fact we can even reduce this to two current sources because of the symmetry in the differential pair. The two current sources are  $I_d$  and  $I_{d3}$ , as indicated in Fig. 6.
- After replacing the current sources  $I_d$  and  $I_{d3}$  with actual current source and current mirrors the design of the OTA become finalized, as depicted in Fig. 7. Note that the transistors  $M_6$  and  $M_9$  provide the current sources,  $I_d$  and  $I_{d3}$ , in the circuit, and  $M_7$  and  $M_8$  are mirroring the current for  $M_9$ . Before we leave this design example notice that the circuit may also need to be biased through the input ports,  $V_1$  and  $V_2$ . In our example  $V_1 = V_{gs1} + V_d$  and  $V_2 = V_{gs2} + V_d$ ; and for each port we need a DC voltage source of about 0.5 V to bias.

Again, for simplicity and brevity purposes the substrate treatment and its biasing have been omitted from our discussion. Also for the reference voltage  $V_B$  usually a separate circuit is designed to provide it for the OTA which is dropped from this study.

As we mentioned earlier, the design is based on 50 nm process and Table 2 provides the components sizes in this process. Table 3, on the other hand, shows the SPICE simulation results for DC analysis of the circuit. For short channel devices BSIM4 and level 14 is used for the MOS transistor models in this design. As expected, the simulation results are in very close agreement with the design criteria.

TABLE 2 – THE OTA COMPONENT SIZES.

| MOS | M1 | M2 | M3  | M4  | M5  | M6  | M7  | M8 | M9 |
|-----|----|----|-----|-----|-----|-----|-----|----|----|
| L   | 2  | 2  | 2   | 2   | 2   | 2   | 2   | 2  | 2  |
| W   | 50 | 50 | 100 | 100 | 100 | 100 | 100 | 50 | 50 |

TABLE 3 - THE DC VOLTAGE SOURCES AND DC CURRENT VALUES IN THE OTA CIRCUIT.

| Source           | VDD | VB    | V1  | V2  | Id1  | Id2  | Id3   |
|------------------|-----|-------|-----|-----|------|------|-------|
| V, $\mu\text{A}$ | 1   | 0.362 | 0.5 | 0.5 | 9.82 | 9.82 | 10.73 |

Next, with the biasing so specified we run the circuit with capacitive load. Figure 8 shows the AC magnitude plot of the

OTA response.

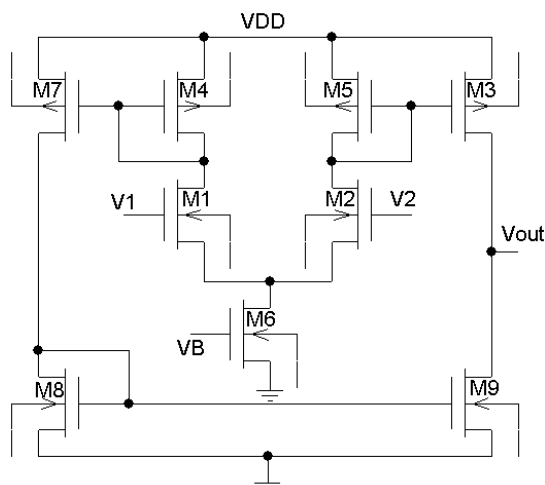


Fig. 7. Final design of the OTA circuit.

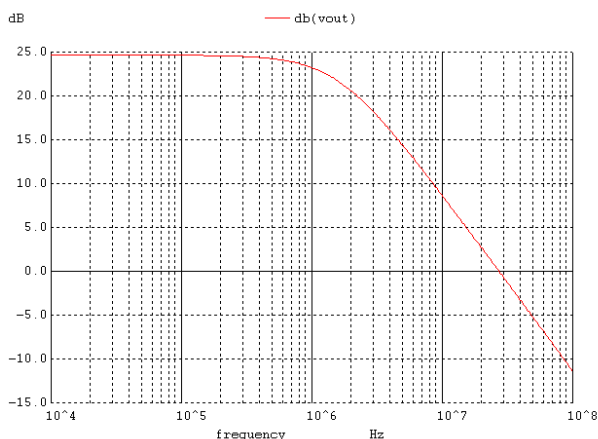


Fig. 8. The AC magnitude and phase response of the OTA

## V. CONCLUSION

A new approach to design of analog integrated circuits is presented. Through local biasing of the transistors we have been able to achieve the desired performance and criteria for the circuit we like to design. The technique is based on designing the core without any external source first and with only sources that are used to locally bias the transistors. Later these sources are transferred to appropriate locations in the core which leads to a new circuit topology and configuration that makes it possible to replace the local biasing sources with final current mirrors and one or two conventional power supplies. Locally biased MOS transistors are introduced and an example of an OTA design is performed.

## REFERENCES

[1] T.L. Pillage, R.A. Rohrer, and C. Visweswariah, "Electronic Circuit & System Simulation Methods," New York, McGraw-Hill, 1995.

[2] J. Vlach, "computer methods for circuit analysis and design," New York, Van Nostrand Reinhold, 1983.

[3] L.W. Nagel, "SPICE2, A computer program to simulate semiconductor circuits," Univ. of California, Berkeley, CA, Memorandum no. ERL-M520, 1975.

[4] Mike Smith, "WinSpice3 User's Manual, v1.05.08", <http://www.ousetech.co.uk/winspice2/>, May 2006.

[5] C.W. Ho, A.E. Ruehli, and P.A. Brennan, "The modified nodal approach to network analysis," IEEE Trans. Circuits Syst., vol. CAS-22, no.6, pp.504-509, June 1975.

[6] C. A. Desoer and E. S. Kuh, Basic Circuit Theory. New York: McGraw Hill, 1969.

[7] Y. Inouea, "Dc analysis of nonlinear circuits using solution-tracing circuits," Trans. IEICE (A), vol. J74 A, pp. 1647-1655, 1991.

[8] \_\_\_\_, "A practical algorithm for dc operating-point analysis of large scale circuits," Trans. IEICE (A), vol. J77-A, pp. 388-398, 1994.

[9] L. B. Goldgeisser and M. M. Green "A Method for Automatically Finding Multiple Operating Points in Nonlinear Circuits," IEEE Trans. Circuits Syst. I, vol. 52, no. 4, pp. 776-784, April. 2005.

[10] R. C. Melville, L. Trajkovic, S.C. Fang, and L. T. Watson, "Artificial parameter homotopy methods for the dc OP problem," IEEE Trans. Computer-Aided Design, vol. 12, no. 6, pp. 861-877, Jun. 1993.

[11] R. Hashemian, "A Methodology to Simulate Circuits with Nonlinear Devices," Proceedings of MWSCAS 2005, Cincinnati, Ohio, August 7 – 10, 2005.

[12] \_\_\_\_, "Partial Local Biasing, a New Method to Modif/Tune Amplifiers for a Desirable Performance", Proceedings of the 2007 IEEE International Conf. on Electro/Information Technology, Illinois Institute of Technology, Chicago, Illinois, May 17– 20, 2007.

[13] \_\_\_\_, "New Analysis and Design Technique for Analog Circuits ", Proceedings of the 2006 IEEE International Midwest Symposium On Circuits And Sys., San Juan, Puerto Rico, August 6 – 9, 2006.

[14] \_\_\_\_, "Analog Circuit Design with Linearized DC Biasing ", Proceedings of the 2006 IEEE International Conf. on Electro/Information Technology, Michigan State University; Lansing, MI, May 7– 10, 2006.

[15] \_\_\_\_, "Designing Analog Circuits with Reduced Biasing Power", the Proceedings of the 13th IEEE International Conf. on Electronics, Circuits and Sys., Nice, France Dec. 10– 13, 2006.

[16] E. Teleo-Cuautle, L.A. Sarmiento-Reyes, "Biasing analog circuits using the nullor concept", Southwest Symposium on Mixed-Signal Design, 2000. SSMDS. 2000.

[17] R. Jacob. Baker, "CMOS, Circuit Design, Layout, and Simulation," 2<sup>nd</sup> ed. Wiley Interscience, 2008, pp. 613 – 823.