

Partial Local Biasing, a New Method to Modify/Tune Amplifiers for a Desirable Performance

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Abstract— A new method is presented for redesigning analog circuits that are facing with response deviation due to component changes or other local variations in the circuit. The method first localizes the problem, i.e., it goes after the components that are causing the problem. If the components involved are nonlinear the method employs a *partial local biasing* on the individual devices until the problem is corrected. The technique used is similar to the local biasing technique [14] where through source augmentation the devices' operating points are modified and adjusted without making any actual changes in the rest of the circuit. Another feature that the method offers is the use of the additivity property, typically used in linear circuits.

Index Terms—Analog circuits, circuit design, circuit simulation, Partial Local Biasing.

I. INTRODUCTION

IN today's fast changing electronic technology, analog and mixed signal integrated circuit techniques have important and decisive place in communication and signal processing. In particular with CMOS technology rapidly embracing the field analog circuit design has become more challenging than ever [1–8]. Other developments in the technology such as lower supply voltages, low-power consumption, performance complexity, and high transistor counts have substantially increased the demand for new design methodologies and techniques.

A major difficulty in dealing with analog circuits is the DC biasing – getting desirable Operating points (OPs) with quick convergence; and the problem is getting worse with the advancement of the technology, due to increase in size and complexity of circuits. Another difficulty dealing with analog circuits is to modify and tune the OPs for desirable operations when some parts in the circuit are modified or replaced by different types.

In fact one of the draw backs in the rapid moving electronic technology is the ability to modify and reuse some of the older but skillfully designed electronic circuits. For example, in the professional electronics as well as in the domestic ones we may often need to modify or exchange the old components in an amplifier with some new ones without changing the basic circuit configuration or the design criteria. There are many reasons for doing so, including the power reduction in the amplifier by reducing the DC voltages, reducing the circuit size, or even to move toward more integration and circuit compactness while keeping the design mostly intact. For example, take the case of a radar system that is still working fine with the old technology. A designer may

be asked to keep the configuration (architecture) and the performance of an amplifier, a modulator or a demodulator intact but change and modernize its components – such as discrete to integrated or BJT to MOS technology – for a better speed or smaller in size. In normal situation changing a component value or exchanging some transistors with another type may significantly alter the original operating regions of the circuit to the level that the circuit loses its normal operation and the responses do not meet the design specifications. Following the traditional methods we may require to perform a series of complete circuit analysis and simulations to correct the problem, and this is especially costly for large and more complex circuits. However, with the proposed methodology it is possible to redesign parts of the circuit without touching the overall structure.

What the proposed methodology offers is to first localize the problem, i.e., go after the components that have been changed and are causing the response deviations. In the second step we separate the linear portion of the circuit from the nonlinear components – the divide and conquer strategy. For the case of a linear component the correction is easy; if the component value has changed we can simply augment the component with a DC source (voltage is series or current in parallel) to compensate for the change so that the change does not (DC-wise) affect the rest of the circuit. However, if the change is due to one or more of the nonlinear components – such as the transistors -- the problem gets more involved and the components need to go through renewed biasing. What is offered here is a method of *partial local biasing* of the components. This is a very important step in redesigning an analog circuit, in a sense that not only we can deal with nonlinear components one at a time, but we also have the freedom to re-bias the components in order to let them operate in our desire regions of operations no matter what the rest of the circuit dictates. It is interesting to note that in this treatment only the nonlinear component is affected by applying *partial local biasing* on it and everything else including the circuit specifications remain unchanged. Another advantage in using this methodology is its linearized behavior, very much like the way linear components behave.

Another important outcome of this methodology is its ability to control and basically reduce the power consumption in a circuit. It is shown that by local biasing the nonlinear devices in a circuit we actually reduce the DC power consumption to its minimum – just enough to get the devices operating in their desired regions [15]. In other words, by locally biasing we are totally cutting off the DC power from

entering the linear elements in the circuit, and hence making the design entirely AC driven and linear.

For education, the impact of the new methodology would be remarkable. It can affect the entire teaching of subjects such as electronic circuits, analog integrated circuits and VLSI designs. For the first time the students can simply assign their biasing choices for each transistor in their design through local biasing [13]. They can then substitute the transistors with their linear models and design their amplifiers totally in the linear environment. In the analysis and simulation domain the students can experience the newly developed *additivity* (linearized behavior) for nonlinear circuits. By applying additivity property the students can play with the old designs but with the new components; freely replace them and if needed apply *partial local biasing* to modify the OPs for better performance. The students can even design their circuit with any component (linear or nonlinear) and do not worry about the biasing part as long as the AC response of the circuit is acceptable. Then they can go to the nonlinear components and modify the biasing regions by applying the *partial local biasing* scheme. The method will allow the students to experiment as to how iterations in a nonlinear circuit can be directed and controlled, and how a possible divergence can be avoided simply by directing the path of convergence. Finally, the students learn how they can design analog circuits with reduced DC power consumptions, as described earlier.

The same impact described for the education is equally valid for the industry in the use of the new methodology. What are particularly important here are the performance and cost effectiveness; and the new methodology offers both. The designer can get the maximum performance because he/she can select the best operating regions for his/her devices independently and before he/she gets engaged with the rest of the design. The method is cost effective because the hardship of dealing with nonlinearity is substantially reduced here, which in turn contributes to reducing the design and development time. This not only reduces the time-to-market for the product but it also reduces the development cost.

The rest of the materials are arranged as follows. Section II of the paper introduces the local biasing and partial local biasing. An algorithm to implement the procedure is provided in this section. In Section III the application of the partial local biasing in modifying and adjusting the biasing of an amplifier is described and some examples are worked out. Finally we conclude the discussion in Section IV.

II. LOCAL BIASING AND PARTIAL LOCAL BIASING

To introduce the local biasing we first need to make some definitions [14].

Null Port: Consider a network N_2 connected to another network N_1 through a port $j(v_j, i_j)$. Port j is null if both current to the port, i_j , and the port voltage, v_j , are zero.

Port nullification: Consider a network N_2 , connected to another network N_1 through a port $j(v_j, i_j)$. Port j is nullified if it is augmented, from both sides (N_1 and N_2), by current sources i_j and voltage sources v_j such that a null port $k(v_k, i_k)$ is created as the result [14].

Local-biasing (LB): By definition, a port is locally-biased if

it is nullified. Likewise, a network is locally-biased if all its ports are nullified. Apparently local-biasing (nullification) of a port is not unique. A port can be locally-biased for any selected OP on its characteristic curve. This is also true for a device.

It now becomes evident that connecting a locally biased device (network) to a powerless network (with no DC supply) does not change the biasing condition of the device. This simply means that, a locally biased device does not need any external DC supply to keep its biasing.

Partial local biasing (PLB): What is meant by partial local biasing is performing local biasing on a device (or a port) without disturbing any other parts in the circuit. Hence, PLB allows a circuit designer to locally change the biasing of one or more nonlinear component in the circuit without causing any (DC-related) disturbance to other parts of the circuit; and this naturally prevents any change in the AC behavior of other components in the circuit, including the output port. PLB is different from LB in the sense that LB makes the entire circuit DC-static (zero DC power) except for the locally biased devices, where as PLB keeps the DC signal values within the circuit intact except it modifies the biasing of the nonlinear device that the PLB is applied to.

PLB has two main properties; it is local and it is not destructive, i.e., it only affects the component behavior and the ac linear model of the devices being under PLB. Second, because of the additivity property applied to PLB, as it was also applicable to LB cases [13], the process of PLB can be gradual and hence simple and directed toward a fast convergence.

A. Locally Modifying/Tuning a Circuit

One of the applications of PLB is to modify or tune a circuit for its optimal performance. This usually happens when a circuit or a system goes through a major revision for component change or in a case of performed some services the circuit may have lost its normal behavior due to changes in the operating regions of its components. PLB may help to redesign, say, an amplifier for better performance without going through an overall design procedure. In all such cases the method allows us to keep the entire circuit unchanged and only modify or tune the biasing of some devices that are not behaving well.

The following algorithm explains the procedure.

1) Algorithm 1:

1. Given a nonlinear circuit – such as an amplifier –, separate the nonlinear devices that require change in their OPs from the rest of the circuit.
2. Take those nonlinear devices one at a time, and for each port of the selected device find the existing OP, say $Q_1(V_1, I_1)$, and then specify the desired OP, say $Q_2(V_2, I_2)$.
3. Find the differences in voltage and current between the two operating points and apply them through augmented voltage and current sources, as specified in Fig. 1. It is important to note that given a device

for adjustment we need to modify all its ports simultaneously. This is because changes in one port in a device (say input) may affect other ports of the same device. In other words, we can isolate the DC operation of a device from the rest of the circuit, but we cannot isolate a port from the other ports in the same device, due to the dependency that exist.

4. Do the preceding operation for other devices in the circuit until all devices are tuned.
5. Continue the design of the amplifier in the linear mode, replacing the linear models of the devices with the old OPs (Q_1) by those with the new OPs (Q_2).
6. In the final stage we can adjust and move the extra supplies that were used (augmented) for PLB to the locations in the circuit that are common for power supplies, for instance, V_{DD} or V_{CC} with a common ground. One way to perform this stage successfully is through source transformation [1-2].

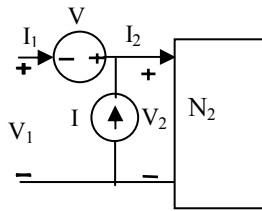


Fig. 1 - A port $j(v_2, i_2)$ of N_2 is augmented to create another port $k(v_1, i_1)$

Another important feature in PLB is its additivity property, typically used in linear circuits. To see this, let us assume that a transistor T_1 , with its OP at $Q_1(V_1, I_1)$ is replaced by another transistor T_2 with a desired OP at $Q_2(V_2, I_2)$. To move Q_1 to Q_2 without affecting the external circuit all we need to do is to augment the port of the new device with a current and a voltage sources $I = I_2 - I_1$ and $V = V_2 - V_1$, respectively. Now, if in another move T_2 is also replaced by a third transistor T_3 with a selective OP at $Q_3(V_3, I_3)$ then we can either augment the port with a current and a voltage sources $I' = I_3 - I_2$ and $V' = V_3 - V_2$, respectively, as indicated in Fig. 2, or we can ignore the other operation and directly replace the initial transistor T_1 by T_3 and use the additivity property to augment the port with $I + I'$ and $V + V'$ sources.

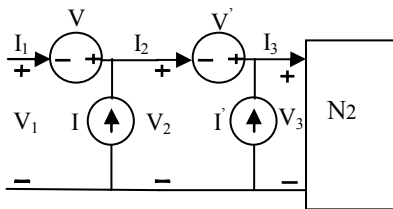


Fig. 2 - A cascaded augmentation of a port in a nonlinear device.

However, the job that still remains to be addressed is to try to combine and move the PLB sources to the desired locations on the circuit configuration, say at V_{DD} and V_{SS} . Although this part of the design still remains to be resolved but methods such as source transformations, the substitution theorem [1], and large sensitivity analysis can be employed to solve the problem. However, it is interesting to note that the process of source transformations and combing sources into one or two power supplies is a linear process.

III. APPLICATIONS AND EXAMPLES

The following example explains some of the issues.

Example 1 - Figure 3 shows part of the circuit of an amplifier, MC1553 [17] with negative feedback. However, due to replacement of some of the original BJTs in the circuit by a different type the biasing of the amplifier is disturbed and, as shown in Fig. 4, the output signal is distorted for a simple sinusoidal input. In trying to remove the distortion, using the traditional procedure – trial and error with global biasing -- it takes six attempts, each time modifying the circuit, until the problem is corrected. In all these attempts the new solutions must be simulated and verified.

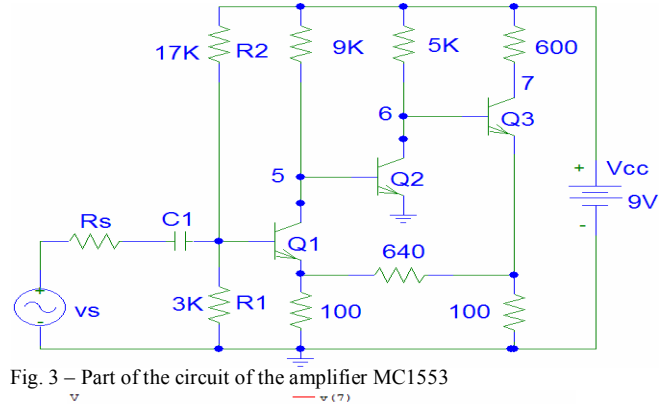


Fig. 3 – Part of the circuit of the amplifier MC1553

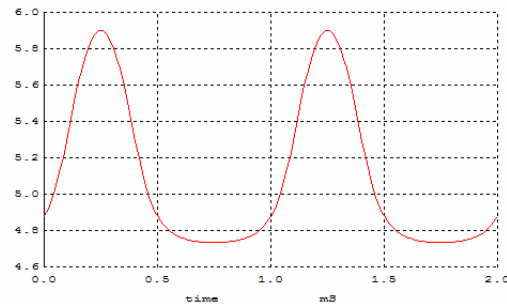


Fig. 4 – The distorted output response.

Alternatively, we try the proposed methodology of PLB. Here we first table the original OPs of the BJTs, as shown in Table I. We notice that Q_2 and Q_3 transistors are doing fine and have remained in their active regions, while OPs for Q_1 are not on the right spots causing Q_1 to fall into the saturation region. Our next attempt is to locally modify the biasing of Q_1

TABLE I
THE FAULTY OPs OF THE BJTs AFTER THE ORIGINAL DEVICES WERE REPLACE BY ANOTHER TYPE

BJT	Q_1	Q_2	Q_3
V_{BE}	6.577551e-01	6.635807e-01	7.049283e-01
V_{CE}	5.341388e-02	1.830471	3.753388
I_B	3.21875e-05	1.05475e-05	4.39711e-05
I_C	9.15721e-04	1.38993e-03	6.86845e-03

to bring it to desired OPs. Table II shows the original biasing of Q_1 vs those selected for the transistor. Note that the last column of the table shows the difference between the two columns indicating the amount of extra sources that must be

augmented to the transistor ports in order to do the biasing modification through the PLB.

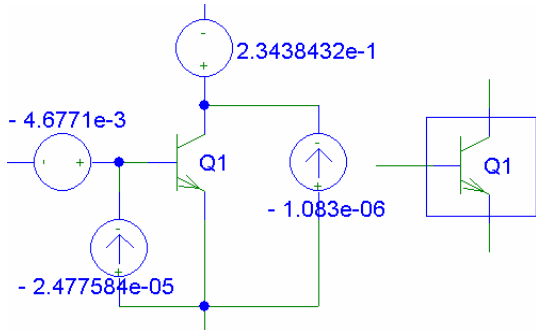


Fig. 5 – The locally biased model of Q1.

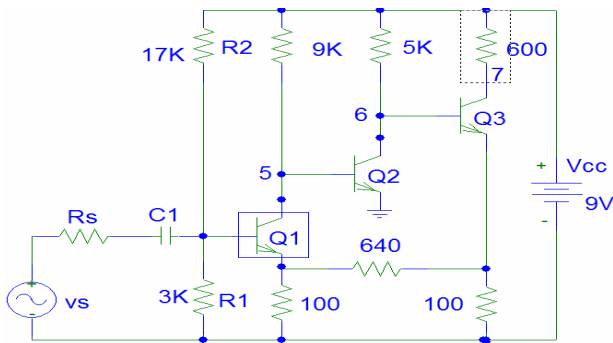


Fig. 6 - Amplifier circuit with Q1 replaced by its new model

Figure 5 shows the transistor Q₁ with the augmented sources attached for PLB; a symbolized Q₁ is also indicated. Figure 6 shows the amplifier circuit where Q₁ is replaced by its modified model (Fig. 5). Finally, we are ready to move the augmented DC sources and combine them with the designated power supplies in the circuit. This is done through source

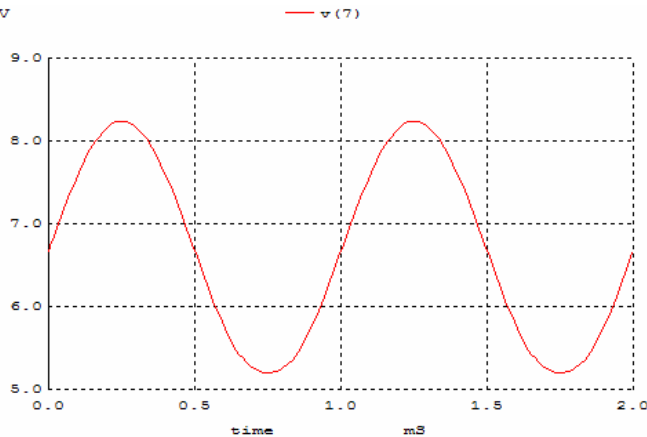


Fig. 7 – The output response of the modified amplifier circuit for the sinusoidal input

TABLE II
LOCAL BIASING OF Q₁ FOR THE ORIGINAL AND THE DESIRED CASES

Q ₁	Original	Desired	Modified
V _{BE}	6.577551e-01	6.530780e-01	- 4.677e-3
V _{CE}	5.341388e-02	2.877982e-01	2.343843e-1
I _B	3.21875e-05	7.41166e-06	- 2.47758e-05
I _C	9.15721e-04	9.14638e-04	- 1083e-06

transformation, Source annihilation, and voltage division techniques – totally linear. In the process of doing this we manage to finalize the circuit configuration by changing R₁ from 3kΩ to 2.89kΩ, and R₂ from 17kΩ to 21.86kΩ. As the result of this OPs modification and after the circuit simulation being performed the output response given in Fig.7. In comparing the waveforms of Fig. 7 with that of Fig. 4 we realize that the distortion has almost vanished.

Example 2 - In this example a well designed npn-pnp BJT feedback amplifier is considered for re-designing. The objective here is to replace the bipolar transistors by their equivalent MOS transistors but keep the design configuration as well as the other component values of the amplifier unchanged. Figure 8 shows the npn-pnp feedback amplifier and Fig. 9 is the amplifier transient response to a sinusoidal input.

In exchanging the BJTs with their MOS counterparts in the amplifier we notice substantial differences in the biasing conditions between the two types. For example, in bipolar transistors we need to provide the DC base current whereas in MOS device the gate biasing current is practically zero, or the base-emitter voltage in BJT is almost constant and equal to 0.7 V, whereas the gate-source voltage in MOS is changing depending on the drain current. In normal biasing situation an overall redesigning of the DC biasing is required for the

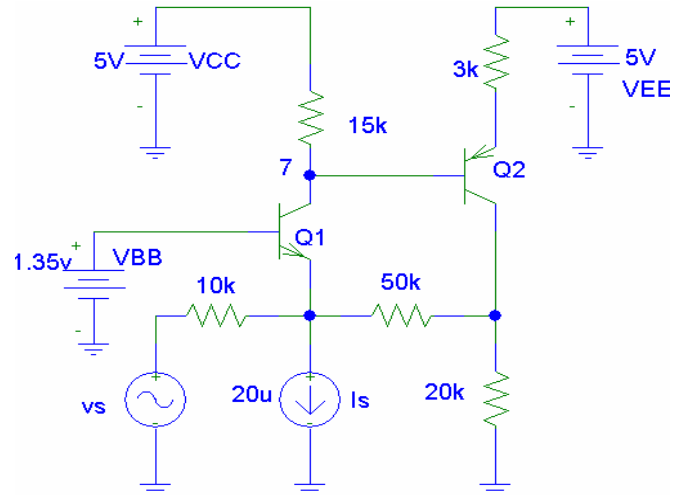


Fig. 8 – The npn-pnp feedback amplifier circuit .

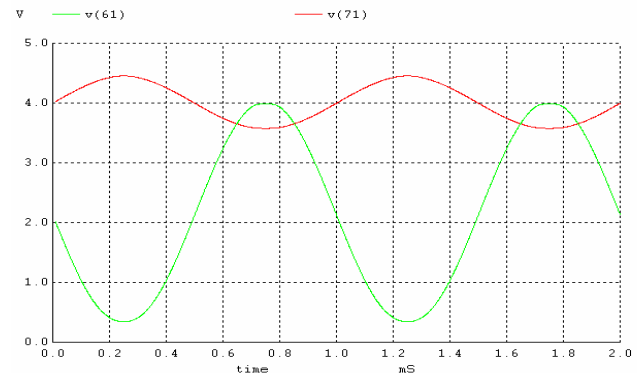


Fig. 9 - The amplifier responses to a sinusoidal input waveform.

amplifier to incorporate the changes; and in doing so we need to go through a number of iterations to find the new OPs for the new devices. The procedure is not only time consuming but we may also need to make substantial changed in some of the component values to get to the right OPs. In case of our proposed methodology, however, we first localize the problem and DC-isolate the transistors from the rest of the circuit. In this example we need to find the biasing conditions of the BJTs and record them first; then take the new MOS devices and assign the desired biasing conditions to them. Next we need to augment the MOS ports with extra current and voltage sources so that the OPs for the MOS transistors move to the right locations on the characteristic curves and, at the same time, no DC variations are noticed in the external circuit. Therefore, not only the problem has broken into much smaller problems (biasing of the individual transistors) but also the other components in the amplifier get immune from any variations as well. The procedure is best explained in the following steps:

- Find the OPs of the BJTs in the existing amplifier and record the biasing values, as indicated in Table III, based on the transistors' locally biased DC-models (see Fig. 5).
- Assign the desired OPs to the new MOS transistors that are going to replace the BJTs in the amplifier. Record the biasing voltages and currents based on the

TABLE III

BJTs OPERATING POINTS FOR THE ORIGINAL AMPLIFIER

	Q ₁	Q ₂
V _{BE}	0.5856	-0.59688
V _{CE}	3.233411	-2.469933
I _B	7.62656e-07	-1.65774e-06
I _C	6.84703e-05	-1.33445e-04

TABLE IV

PROPOSED LOCAL BIASING OF M₁ AND M₂ TRANSISTORS, AND THEIR DIFFERENCES WITH THE BJTs BIASING VALUES.

	M ₁	M ₂	Q ₁ - M ₁	Q ₂ - M ₂
V _{GS}	1.947113	-1.697185	-1.3615139	-1.100306
V _{DS}	1.896731	-2.664088	1.33668	-0.194155
V _{SB}	--	--	--	--
I _D	1.367e-04	-1.177e-04	-6.822e-05	-1.57e-05

MOS transistors' locally biased DC-models, as shown in Table IV.

- Locally bias the MOS transistors by augmenting their ports with current and voltage sources that their values are the differences between the biasing conditions of the BJTs and the MOS transistors. Table IV provides these differences in biasing, and Fig. 10 shows the PLB for M1 and M2 transistors.
- Apply source transformation to move the augmented sources to the designated locations in the amplifier circuit. Figure 11 shows the amplifier redesigned by MOS transistors substituted for the BJTs. Note that the augmented current and voltage sources are moved and the result has cause changes in supplies VBB

from 1.35 V to V_{GG} = 3 V, and I_S from 20 μA in the bipolar amplifier to 50 μA the MOS amplifier.

Figure 12 shows the transient response of the modified MOS amplifier to a sinusoidal input. When compare with the response from the original bipolar amplifier, Fig. 9, we clearly see the similarity between the two and with no distortion; the only noticeable difference between the two cases is that the voltage gain in the MOS amplifier shows about 42% lower that that in the bipolar transistor amplifier which is normal by considering the fact that the original circuit was aimed at BJT

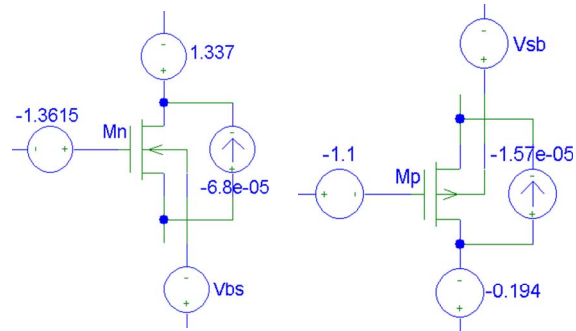


Fig.10 - Partial local biasing of the MOS transistors.

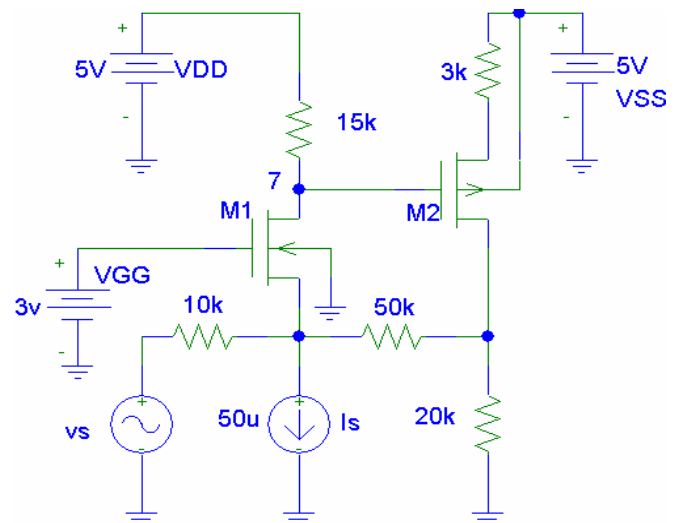


Fig.11 - Partial local biasing of the MOS transistors.

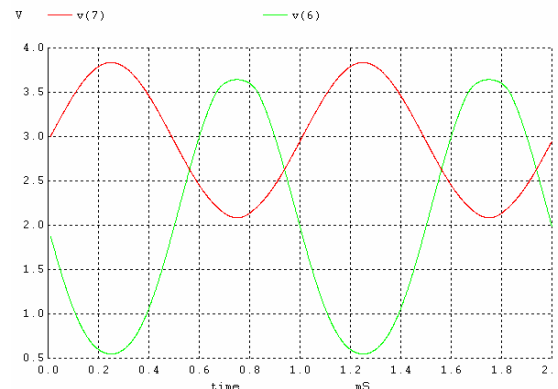


Fig.12 - MOS amplifier response to a sinusoidal input.

amplifier. However, there are other features that have been substantially improved in the new design. For instance the new design shows much higher input impedance, and hence

higher current gain, than the original design.

IV. CONCLUSION

A new methodology is introduced in this presentation that substantially simplifies the biasing or re-biasing of nonlinear devices in an analog circuit. The method first localizes the problem, i.e., it goes after the components that are causing the problem. If the components involved are nonlinear the method employs a *partial local biasing* on the individual devices until the problem is corrected. The technique used here is very similar to the local biasing technique except it does not disturb the rest of the circuit. Two examples are provided. Example 1 show how a deviation in the biasing of a circuit, caused by a change in the characteristic of a transistor, is corrected through PLB; and Example 2 shows that how both BJTs in a feedback amplifier are replaced by MOS transistors and how the biasing is modified for the new design such that the output waveforms are not distorted.

REFERENCES

- [1] T.L. Pillage, R.A. Rohrer, and C. Visweswariah, "Electronic Circuit & System Simulation Methods," New York, McGraw-Hill, 1995.
- [2] J. Vlach, "computer methods for circuit analysis and design," New York, Van Nostrand Reinhold, 1983.
- [3] L.W. Nagel, "SPICE2, A computer program to simulate semiconductor circuits," Univ. of California, Berkeley, CA, Memorandum no. ERL-M520, 1975.
- [4] Mike Smith, "WinSpice3 User's Manual, v1.05.08", <http://www.ousetech.co.uk/winspice2/>, May 2006.
- [5] C.W. Ho, A.E. Ruehli, and P.A. Brennan, "The modified nodal approach to network analysis," IEEE Trans. Circuits Syst., vol. CAS-22, no.6, pp.504-509, June 1975.
- [6] C. A. Desoer and E. S. Kuh, Basic Circuit Theory. New York: McGraw Hill, 1969.
- [7] Y. Inouea, "Dc analysis of nonlinear circuits using solution-tracing circuits," Trans. IEICE (A). vol. J74 A, pp. 1647-1655, 1991.
- [8] ____, "A practical algorithm for dc operating-point analysis of large scale circuits," Trans. IEICE (A), vol. J77-A, pp. 388-398, 1994.
- [9] L. B. Goldgeisser and M. M. Green "A Method for Automatically Finding Multiple Operating Points in Nonlinear Circuits," IEEE Trans. Circuits Syst. I, vol. 52, no. 4, pp. 776-784, April. 2005.
- [10] R. C. Melville, L. Trajkovic, S.C. Fang, and L. T. Watson, "Artificial parameter homotopy methods for the dc OP problem," IEEE Trans. Computer-Aided Design, vol. 12, no. 6, pp. 861-877, Jun. 1993.
- [11] R. Hashemian, "A Methodology to Simulate Circuits with Nonlinear Devices," Proceedings of MWSCAS 2005, Cincinnati, Ohio, August 7 – 10, 2005.
- [12] ____, "Use of Conditional Additivity in Circuits with Exponential Nonlinearities," Proceedings of MWSCAS 2005, Cincinnati, Ohio, August 7 – 10, 2005.
- [13] ____, "New Analysis and Design Technique for Analog Circuits ", Proceedings of the 2006 IEEE International Midwest Symposium On Circuits And Sys., San Juan, Puerto Rico, August 6 – 9, 2006.
- [14] ____, "Analog Circuit Design with Linearized DC Biasing ", Proceedings of the 2006 IEEE International Conf. on Electro/Information Technology, Michigan State University, Lansing, MI, May 7– 10, 2006.
- [15] ____, "Designing Analog Circuits with Reduced Biasing Power", the Proceedings of the 13th IEEE International Conf. on Electronics, Circuits and Sys., Nice, France Dec. 10– 13, 2006.
- [16] E. Teleo-Cuautle, L.A. Sarmiento-Reyes, "Biasing analog circuits using the nullor concept", Southwest Symposium on Mixed-Signal Design, 2000. SSMSD. 2000.
- [17] A. S. Sedra, and K. C. Smith, Microelectronic Circuits. New York: Oxford University Press, 2004.