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A Linear-like Biasing Technique for Nonlinear Circuits

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Abstract— A new biasing technique is introduced for complex analog circuits. The technique is gradual, controllable and fast converging. The technique offers the circuit designers to initially and directly choose the devices operating points first and then proceed for designing linearly. The technique is based on a local biasing method that removes all DC supplies from the circuit and replaces them by sources augmented to the ports of the devices so that the ports are DC-nullified. It is shown that when the local biasing is done in steps the additivity property, used in linear circuits, can be implemented. Finally, the local biasing makes the nonlinear devices to respond to an AC signal, at selected operating points, just like other linear elements without any need of externally bias them.

Index Terms—Analog Circuits, Circuit Design, Local Biasing, Simulation.

I. INTRODUCTION

The main difficulty dealing with nonlinear circuits is the biasing, i.e. getting desirable operating points with fast convergence; and the problem is getting worse with the advancement in the analog technology. The analysis of such circuits may even lead to multiple DC operating points [1, 5], or causing instability because of the existence of positive feedbacks in the circuit [3]. SPICE circuit simulator uses methods such as Newton-Raphson iteration techniques [2] for allocating operating points, but the problem still remains for more complex circuits to get them converge. Techniques such as changing the tolerance values, adding minimum conductances (GMIN) and shunt resistors to the circuit, as well as supply stepping are typically adopted in SPICE to make the circuit to converge.

There are numerous causes for these problems. One difficulty stems from the fact that in the traditional method an analog circuit is usually analyzed and simulated as whole – linear and nonlinear components all together. This certainly makes quick and smooth convergences difficult for large circuits. In addition a poor selection of the initial conditions plus large and unregulated steps of iterations can cause the circuit to diverge. An additional difficulty may result from a fixed circuit configuration. For instance, applying the DC supplies in certain pre-assigned locations may not always be the best choice, and floating them first may result in a better biasing and quicker convergence. For the final supply locations we can always use methods such as source transformation to move the floating sources to appropriate locations in the circuit without altering the circuit criteria. Another problem with the global biasing is that it cannot address local changes and modifications. For example, if some operating points do not meet the design criteria or a few components are replaced during the design the circuit needs to go through the entire biasing process again.

The purpose here is to develop a new methodology that helps to divide an analog circuit into its linear and nonlinear parts, and exert more control on the performance of its nonlinear components for a fast and desirable response. The objective is to introduce a new biasing scheme that only deals with nonlinear components individually. In the circuit analysis and simulation what it means is to gradually replace the DC supplies by building up the biasing sources around the individual nonlinear devices. It is shown that a very powerful and unique additivity property helps us to perform this operation smoothly and effectively. In the case of circuit design we can even start from "local biasing" of nonlinear devices and direct the design entirely into the linear domain for the rest of the process. The major problem here is that the DC supplies become distributed, and often in non conventional locations. To take care of this we need to use techniques such as source transformation to bring them together and possibly replace them by conventional supplies such as V_{DD} or V_{CC}. In addition, because the proposed method offers a complete isolation of individual nonlinear devices, it makes it possible to locally modify, adjust and tune the circuit without disturbing the rest of the circuit. This feature is interesting and useful for designs that need partial modifications, such as changing the transistors in an amplifier to different types.

Another important outcome of this methodology is that it offers a new look at the DC power distribution within a circuit, and it offers an ability to control and reduce the DC power consumption. It is shown that by local biasing of the nonlinear devices we actually reduce the DC power to its minimum in the circuit – just enough to get the devices biased. In other words, by locally biasing we are totally removing the biasing (DC) currents from entering the linear elements in the circuit, and hence making the design entirely AC and linear.

II. LOCAL BIASING

To introduce local biasing we need to introduce port augmentation and port nullification.

A port $j(v_j, i_j)$ of a network N_2 with current i_j and voltage v_j, is said to be *augmented* by a current source I and a voltage source V if i) a current source I is added across the port, and ii) a voltage source V is added in series with the port, as shown in Fig. 1. Another port $k(v_k, i_k)$ is created as the result. Then port $k(v_k, i_k)$ is *nullified* if $I = i_j$ and $V = v_j$, resulting in v_k and i_k being equal to zero.

A network with m ports is *locally biased* if all its m ports are nullified.

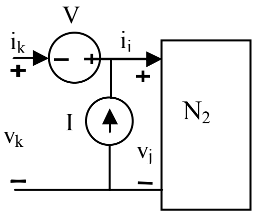


Fig. 1 - A port $j(v_j, i_j)$ of N_2 is augmented to create another port $k(v_k, i_k)$

Now we can introduce the concept of additivity in nonlinear circuit analysis through the port nullification. Consider a one port network N_2, shown in Fig. 2(a), with its port characteristic curve shown in Fig. 2(b); and let Q(V, I) be an arbitrary operating point on the characteristic curve. Next, we augment port j by a current source I and a voltage source V to generate a new network N'_2 with a port $k(v_k, i_k)$, as shown in Fig. 2(c). Evidently, port k is nullified and its characteristic curve is identical to that of port j except for the v and i axis that have moved to point Q, as shown in Fig. 2(d). Next we can simply bias N'_2 via a network N_1 and its port k as if N'_2 has the i-v characteristic curve shown in Fig. 2(d). Now after apply the new biasing network, N_1, the new operating point has moved to Q' on the characteristic curve. Hence, we have been able to reallocate the i-v coordinates to place the origin on a desired location on the characteristic curve first and then search for a new operating point. This leads to the next important theorem.

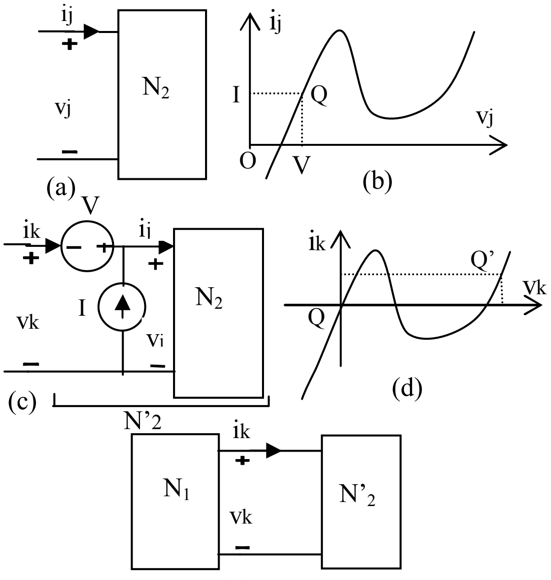


Fig. 2 - (a, b) A one-port network with its port characteristic; (c, d) port k after being augmented and; (e) the augmented port driven by N_1

Theorem 1 – Additivity in nonlinear biasing: Consider a network N_2 connected to another network N_1 through a port; and let N_1 contain n DC supply sources. Group the sources arbitrarily into p mutually exclusive groups. Then the total effect of network N_1 on N_2, due to all n supplies in N_1, can be determined by adding p times the effect of N_1 on N_2, where each time a) only one group of sources in N_1 is applied, and b) the port is nullified before the next operation is performed.

Evidently Theorem 1 can be extended to include multiple-port networks as well, which leads to the following corollary.

Corollary 1 – Additivity in m-port nonlinear biasing: Consider a network N_2 connected to another network N_1 through m ports, and let N_1 contain n DC supply sources. Group the sources arbitrarily into p mutually exclusive groups. Then the total effect of network N_1 on N_2, due to all n supplies in N_1, can be determined by adding p times the effect of N_1 on N_2, where each time a) only one group of sources in N_1 is applied, and b) all m ports are nullified before the next operation is performed.

As stated, the proposed additivity property offers a novel and remarkable methodology for nonlinear circuit analysis, which is similar to the superposition property used in linear circuits. In addition, this additivity property can provide a simple mechanism through which we can gradually and arbitrarily build up the local biasing of nonlinear devices in the circuit, replacing the regular DC supplies, until we are satisfied. Likewise, in design we can start from local biasing the devices and augment their ports with V and I sources so that they operate in desirable operating regions. The rest of the design is dealing with a linear circuit replacing the devices by their linear models. Finally, we may need to apply certain source transformation techniques to move the local biasing (augmented) sources to proper locations in the circuit, such as to V_{DD} and V_{SS}. There are number of methods known for source transformations [1], and the idea here is to minimize the number of supplies finally left in the circuit.

III. ANALYSIS AND SIMULATION

The method discussed so far can be implemented on any nonlinear circuit. In case multiple numbers of devices are used in a circuit we can identify each nonlinear device with its distinct ports and deal with the collection of the devices as an m-port nonlinear network. The following algorithm describes the steps necessary to analyze and simulate an m port nonlinear circuit, implementing the new methodology.

A. Algorithm 1:

i) Given a nonlinear circuit we first identify all nonlinear devices through their ports and group them into one nonlinear network N_2 with m ports, $j(v_j, i_j)$, for j = 1, 2, …, m, connected to the rest of the circuit, N_1.

ii) Group the DC supplies in N_1 in such a way that applying them in a sequence best performs the local biasing of N_2, and it possibly guaranties quick convergences. This is a crucial step and needs some design experiences to achieve a good result.

iii) Keep the first group of supplies in N_1 and remove the rest. Assume that this group makes N_2 to operate at $Q_1(V_1, I_1)$ on the characteristic curve (for simplicity only one port is considered which can be extended to m). Next, augment the port with I_1 and V_1 sources and remove the first group of supplies from N_1. This will create a nullified port.

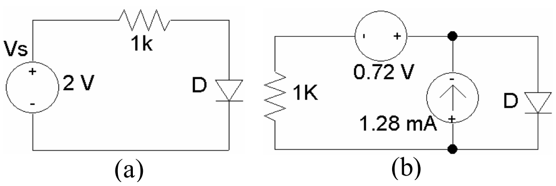
iv) Introduce the second group of supplies into N_1 now with other sources still removed. Suppose this causes the operating point to move from $Q_1(V_1, I_1)$ to $Q_2(V_2, I_2)$ on the characteristic curve. Next add the augmented sources I_2 to I_1 and V_2 to V_1 and remove the second group of supplies from N_1. This again causes the port to nullify. Continue the procedure for other groups of supplies until all other groups are successively applied. Due to the additivity property (Corollary 1), the port is now augmented with one current source and one voltage source that each is the accumulation of the currents or voltages applied for local biasing during the consecutive operations.

v) Finally, the circuit is biased and it -- N_1 connected to N_2 -- is ready to perform AC analysis. As stated earlier, in the case of local biasing the circuit responses to AC signals remain entirely AC without being mixed with any DC components.

B. Implementation:

We are now ready to implement the technique and algorithm for biasing nonlinear circuits such as amplifiers. Within the three major semiconductor devices, diodes, bipolar and MOS transistors, p-n junction diodes are considered one-port devices. BJTs are typically considered two-port devices, but they can be turned into two one-port devices if *Ebers-Moll* large signal model is used. MOS transistors are three-port devices; however, we notice that the DC currents through the gate and substrate ports are ignored and hence we need only four sources to locally bias an MOS. The four sources are: I_D and V_{DS} to nullify the drain-source port, V_{GS} and V_{BS} to nullify the gate-source and the substrate-source ports, respectively.

Example 1 – Diode Circuit: Figure 3(a) shows a simple diode circuit connected to 2 V DC supply through a 1 K-ohm resistor. The experiment shows that the current through the diode in this situation is I_D = 1.28 mA and the voltage across the diode shows V_D = 0.72 V. Now, if we locally bias the diode by a current source 1.28 mA and a voltage source 0.72 V the current through the 1 K-ohm resistance becomes zero, and this is contrary to the case in Fig. 3(a), where the current through the 1 K-ohm resistance is 1.28 mA. This is because the diode port in Fig. 3(b) is nullifies. Another important result obtained here is that in local biasing the DC power loss is limited to the nonlinear devices (diode in here) only; therefore, local biasing minimizes the DC power loss in the circuit.



(a) (b)

Fig. 3 – Diode circuit, (a) global biasing, and (b) local biasing.

Example 2 –BJT Circuit with multiple operating points: The circuit shown in Fig. 4 is very much similar to the one reported by Goldgeisser and Green [3] to have nine operating points. To compare the normal method of analysis with ours we first simulate the circuit with all three external supplies, 12V, 10V and 2V, being simultaneously applied to the circuit. We use WinSpice3 for the simulation and to reduce the effect of other factors in the convergence problem we disabled the source stepping and the shunt convergence aid through the choice of OPTIONS: ITL6=1 and MINCONVSHUNT=0. It is shown that it takes 163 iterations for the transistors to converge to a set of operating points, and Table I shows the circuit node voltages at this converged operating point.

Alternatively we are going to use the proposed local biasing methodology as described in Algorithm 1. First, we group all four BJTs in the circuit as an 8-port nonlinear circuit N_2. Next, within different grouping schemes of the DC supplies we specify them into two groups, the 12V and 10V, and the 2V, in the linear portion of the circuit, N_1. Initially we keep the 12V and 10V supplies in the circuit and remove the 2V. Now we simulate the circuit by using WinSpice3 with the same conditions as before. The circuit converges quickly to a set of operating points. We then remove the 12V and 10V supplies from the circuit, and locally bias the transistors accordingly (Algorithm 1). This completes the first step. In the next step we add the 2V supply to the circuit and simulate the circuit again. After a few iterations the circuit converges to a new set of operating points. Evidently these new operating points must be the same as the ones obtained in the earlier method. Finally, we use the additivity property adding up the augmented sources (V sources together and I sources together) in order to get the final local biasing sources.

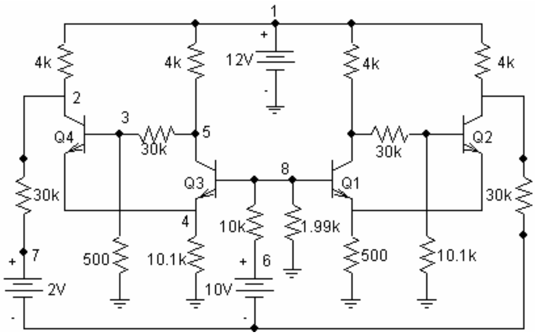


Fig. 4 – A BJT circuit with multiple operational points

Table II provides the augmented voltage and current supplies used during two steps of local biasing. Note that the values in the column 5 are the sum of the corresponding values in the columns 3 and 4, which again proves the validity of the additivity property in local biasing. Figure 5 represents the modeling scheme of an npn transistor when locally biased, a transistor symbol when locally biased is also shown. Figure 6 depicts the circuit (Fig. 4) when it is locally biased.

TABLE I - THE CIRCUIT NODE VOLTAGES FOR FIGURE 8 EXTERNAL BIASING

V(2)	V(3)	V(4)	V(5)	V(8)
10.425	0.171	0.5216	10.428	1.0967

TABLE II - VOLTAGE AND CURRENT SUPPLIES USED FOR LOCAL BIASING

BJT	BJT Ports	12V and 10V	2V	All Supplies
Q_1	V_{BE1}	0.667	-0871	-0.204
	V_{CE1}	4.17	5.35	9.52
	I_{B1}	1.18e-05	-1.18e-05	-1.61e-12
	I_{C1}	1.63e-03	-1.63e-03	1.24e-11
Q_2	V_{BE2}	0.437	0.248	0.685
	V_{CE2}	9.66	-9.61	5.16e-02
	I_{B2}	7.09e-09	9.79e-05	9.79e-05
	I_{C2}	2.48e-07	2.50e-03	2.50e-03
Q_3	V_{BE3}	0.589	-0.014	0.575
	V_{CE3}	9.40	0.51	9.91
	I_{B3}	8.80e-07	-3.27e-07	5.53e-07
	I_{C3}	8.80e-05	-3.69e-05	5.11e-05
Q_4	V_{BE4}	-0.728	0.377	-0.351
	V_{CE4}	9.58	0.32	9.90
	I_{B4}	-1.71e-12	1.09e-14	-1.70e-12
	I_{C4}	1.26e-11	3.46e-13	1.30e-11

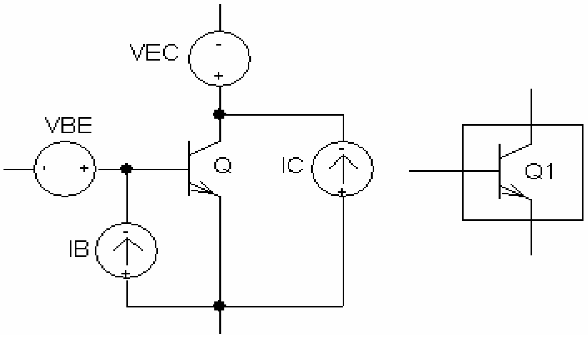


Fig. 5 - The local biasing scheme and the symbol for an npn transistor.

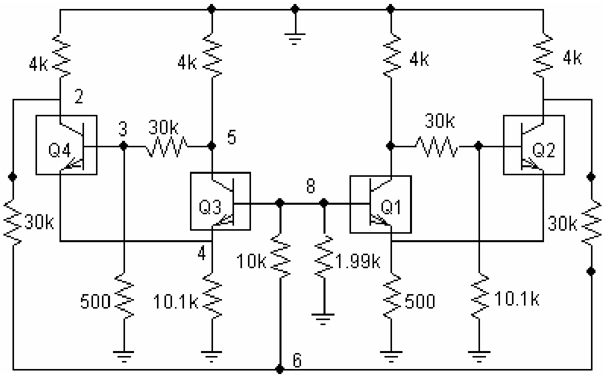


Fig. 6 - The BJT circuit with locally biased transistors

In comparison, we notice that while by using the traditional method it takes 163 iterations for the circuit to converge but it only takes 10 iterations and in two steps to converge to the same locations when we use the proposed method. This is certainly an outstanding achievement in the analysis and simulation of complex circuits. An important reason for this highly effective biasing strategy is the power of maneuvering that it provides to a circuit designer. The local biasing, being additive, give us the choice of not only grouping the DC supplies but also the freedom to successively apply them the way we want, and add up the result at the end. For example in this circuit if we apply the "2V" supply first and the "12V and 10V" supplies second the number of iterations would substantially increase. This simply suggests that not any arbitrary grouping and sequentially applying the supplies provides a good result. In fact experiences and skills in analog circuit design play an important rule in optimizing the procedure.

IV. CIRCUIT DESIGN

Local biasing brings the circuit design into a new light, where a designer can start from his/her own choice of operating points for the devices and do the rest of the design linearly. Another reason that local biasing helps for better design is that in the local biasing the coordinates are moved to the operating points of our choice on the characteristic curves, so that the AC signal doesn't mix with any DC, where as in the traditional case the (global) biasing both signals are mixed and they normally get separated only through the use of extra components such as coupling capacitors. Finally, local biasing has a profound effect on reducing the DC power consumption and in cases of complete local biasing this power loss gets to its absolute minimum. In addition, lowering the power loss has other advantages such as making the design more efficient, lowers the noise, and improves the overall performance of the circuit.

V. CONCLUSION

A new methodology is introduces her that removes the burden and simplifies handling the nonlinearities in analog circuit biasing. The key concepts in this development are port nullification and additivity. The additivity is particularly helpful in selectively and sequentially applying the DC sources to get operating points smoothly and quickly. In an example it is shown that while it takes 163 iterations for a circuit to converge to an operating point by using the traditional method it takes only 10 iterations to converge to the same operating point when the new methodology is used. There are also merits in the new technique in simplifying and basically linearizing the circuit design. DC power management and power reduction is another area that this methodology addresses. An analog circuit simply consumes minimum DC power when it is locally biased.

VI. REFERENCES

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