New Analysis and Design Technique for Analog Circuits

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Abstract—**Desirable biasing of nonlinear devices in an analog circuit is an essential step and often difficult. The difficulty comes from the fact that for biasing nonlinear devices we need to go through an iteration procedure that is usually timely and may end up with divergence. A new methodology is presented here that completely removes the nonlinearity of the biasing in a design procedure. The method also simplifies the analysis by using the "additivity" property, typically used in linear circuits. The method focuses on *local biasing* using a port nullification technique that isolates the nonlinear devices from the linear portion of the circuit. This method allows a circuit designer to select his/her desired operational regions for the nonlinear devices, and start working on the rest of the (linear) circuit avoiding biasing iterations or even a possible divergence.**

I. Introduction

Finding the DC operating points (OPs) of nonlinear devices in a circuit is important for the design of analog circuits. However, the job becomes difficult and often complicated for sizable circuits, particularly those with positive feedbacks where the chance for the OP being unstable is quite high. In some advanced circuit simulators, such as SPICE [1], methods based on Newton-Raphson iteration techniques are typically employed. However, the major difficulty in such methods is the circuit convergence, and the number of iterations that usually needed to get close enough to the desired OPs. The problem usually arises from applying the entire DC sources at once and with a poor selection of the initial conditions for the OPs. Large and unregulated steps in search for OPs increase the chances of going out of range, and ultimately ending with non-convergence [2 - 8].

What we present here is a procedure that allows controlling the search for OPs, and with a more gradual manner. It enables the circuit designer to select different regimes of applying supply sources to a nonlinear circuit in order to achieve a quick convergence. In this technique the designer groups the supplies, prioritizes them, and applies them in a manner that leads to desired OPs. In short, with this technique the circuit designer has tremendous power to control the nonlinear behavior of the circuit by adopting a *supply sequencing* that even makes it possible to split DC sources, group them and do different combinations that leads to less iterations and quick convergence.

The key concept that makes all this possible is the additivity property, widely used in linear circuits [9], the only difference here is conditioning, or partial local biasing, the ports for the next step. The way it is done is to record the intermediate OPs that are found in each operation and use them as the starting points (the origins of the nonlinear v-i characteristics) for the next operation. This continues until all sources are used and the final OPs are gradually moved to their destinations. The method uses two close concepts: i) *Port Nullification*, and ii) *Network Inactivation*, as will be discussed.

II. Port Nullification

To simplify our discussions we consider the following assumptions and definitions throughout the article:

Networks are assumed to be *memoryless* and they can be linear or nonlinear. The term *powerless* is referred to a network that has no internal supply and no dependent source exist in the network that is controlled by an external signal. A *null* network is referred to a network with no element; leaving the port nodes either open circuited or sort circuited. A port $j(v_j, i_j)$ of a network N_2, characterized by current i_j and voltage v_j, is *augmented* by a current source I and a voltage source V if the sources are added to the port as specified in Fig. 1.

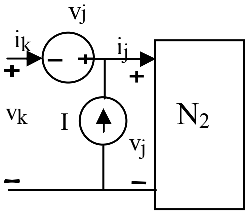

Figure. 1 - port $j(v_j, i_j)$ of N_2, augmented to create another port $k(v_k, i_k)$.

Null Port: Consider a network N_2 connected to another network N_1 through a port $j(v_j, i_j)$, as shown in Fig. 2. port j is *null* if both i_j and v_j are zero.

Evidently, when a port is null it is null with respect to both networks, N_1 and N_2, and either network can be a null network.

Property 1: Consider two networks N_1 and N_2 connected together through a port j. If port j is null then the v-i characteristic curve of the port, looking through either networks, passes through the origin and the origin is the OP for that port.

The proof follows from the definition of the null port.

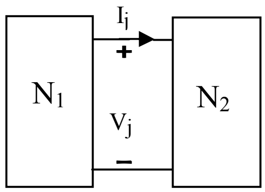

Figure. 2 - A *null* port representation.

Port nullification: Consider two networks N_1 and N_2 connected together through m ports $j(v_j, i_j)$, for j = 1, 2, …, m. Port j is nullified if it is augmented from both sides (N_1 and N_2) by current sources i_j and $-i_j$, and voltage sources v_j, as shown in Fig.3 for a port j. Evidently it results in the creation of m null ports $k(v_k, i_k)$, for k = 1, 2, …, m.

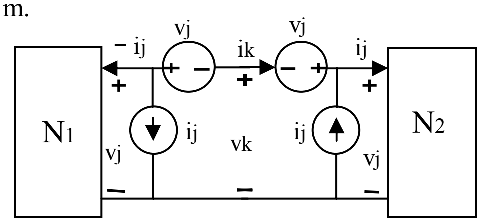

Figure 3. Port nullification procedure.

Property 2: Port nullification only stops the flow of DC power (current and voltage) flowing from one network to the other and it does not affect the flow of AC signal.

Property 2 shows that through nullification we can separate between DC and AC analysis of networks, and hence from now on our discussion will only be about DC biasing.

Property 3: Consider a network N_2 connected to another network N_1, through one or more ports. If all the ports are nullified, removing all sources from N_1 (including any dependencies to external signals) has no effect on N_2. This, therefore, provides an alternative method to nullify ports of a network, as shown in Fig. 4.

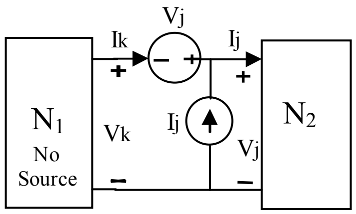

Figure. 4 – An alternate *Port Nullification*.

The proof of Property 3 is quite evident. First we must notice that connecting a nullified port to another notified port does not make any change in either port (network). Second, removing all supply sources from a network makes its ports nullified.

Note from Property 3 that the network N_1 can become a null network. Therefore, if all the ports in N_2 were nullified, removing the entire network N_1 and leaving the null ports of N_2 open circuit (or short circuit) would not affect N_2.

Local Biasing: By definition, a port is locally biased if it is nullified. Likewise, a network is locally biased if all its ports are nullified.

It now becomes evident that connecting a locally biased device (network) to a powerless network does not change the biasing condition of the device.

Example 1: Consider the circuit of Fig. 5(a), where two parts of a circuit are connected through a port $j(v_j, i_j)$. Suppose the MOS diode M_1 is characterized by $i = K(v-1)^2$ mA, for v > 1V, and let $K = 0.5$ mA/V^2. The analysis shows that port j is not a null port, since $I_j = 1$ mA and $V_j = 3$ V. Next, we augment port j by current and voltage sources I_j and V_j, from both sides, to create a null port $k(v_k, i_k)$, as shown in Fig. 5(b). Note that, although the i–v characteristic curve for port j does not pass through the origin but that of port k does. It is important to note that port k belongs to both networks N_1 and N_2, and therefore, its characteristic curve looking to network N_1 must pass through the origin as well (Property 1). Because N_1 is a linear resistive circuit this simply means that a single resistance can model N1, looking through port k. To find such equivalent resistance we remove all sources from N_1 and evidently this source removal has no effect on N_2, as shown in Fig. 5(c).

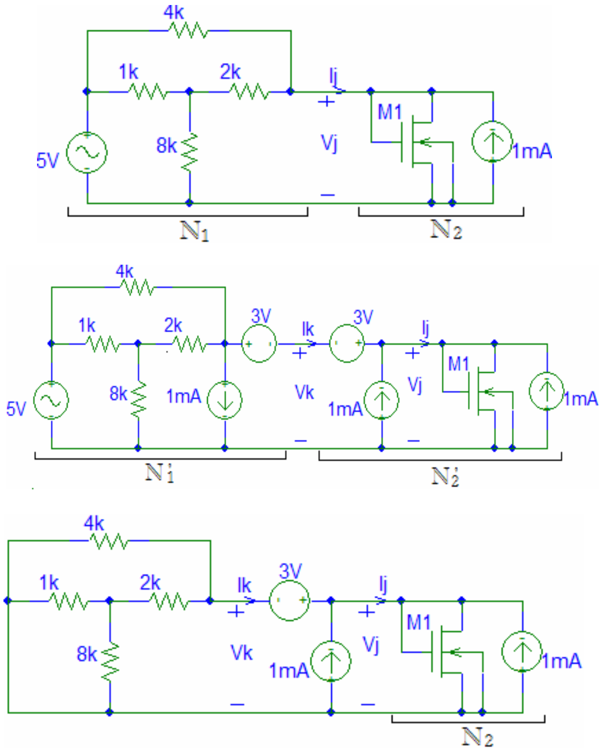

Figure. 5 – (a) Two networks N1 and N_2 separated by port j, (b) and (c)

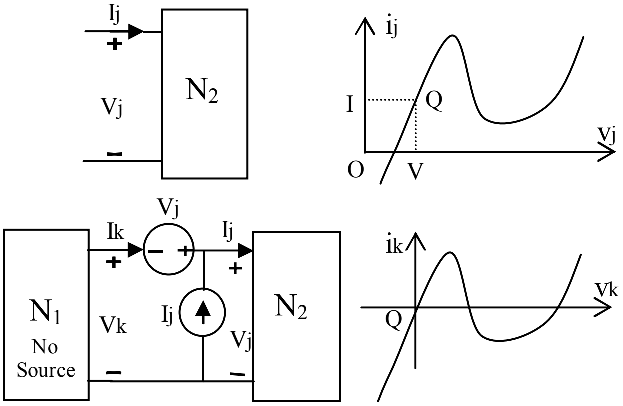

Figure.6- (a, b) A network with its port characteristic, (c, d) port k after being nullified.

Consider a network N_2 with its port characteristic curve given in Figs. 6(a) and (b), and let Q (V, I) be a point on the port's characteristic curve. From the definition of *port nullification* it follows that the newly generated port $k(V_k, I_k)$, connecting N_2 to a powerless network N_1, is nullified if port $j(V_j, I_j)$ is augmented by a current source I and a voltage source V, as shown in Fig. 6(c). It is also evident from Property 1 that both ports j and k have the same v-i characteristic curve, except that in the case of port k the coordinates have moved to a new position with Q point becoming the origin, as indicated in Fig. 6(d).

Now, if we add DC sources to N_1, then N_1 biases N_2, through port k as if N_2 had the v-i characteristic curve given in Fig. 6(d). This leads to the next important theorem, with the proof being omitted.

Theorem 1:- General-Additivity: Consider an m-port network N_2 connected to another network N_1 containing DC supply sources. Group the sources in N_1 into n mutually exclusive groups. The total effect of network N_1 on N_2 due to all sources in N_1 can be determined by adding n number of times the effect of N_1 on N_2, where a) each time a different group of sources is used in N_1 and b) the ports in N_2 are nullified each time before the operation is performed.

III. Implementation and Example

The method discussed so far can be implemented on any nonlinear circuit or device. If, however, multiple number of nonlinear devices are used in a circuit we can handle the case in two different ways. One method is to take each nonlinear device as a separate entity and deal with it as a nonlinear network. The second method is to group parts (or all) of nonlinear devices into nonlinear network and handle the group collectively. Although the later method shows some merit, but because of certain complexities involved we only consider the former case here, i.e., we deal with nonlinear devices individually in this article.

Within the three major semiconductor components, diodes, BJT and MOS, p-n junction diodes are one-port devices. BJTs are typically two-port devices, but they can be turned into two one-port devices if *Ebers-Moll* large signal models are used [10]. MOS transistors are considered three-port devices, but it is shown that four sources are sufficient to nullify all three ports. For the drain-source port we need to nullify I_D and V_{DS}. For the gate-source we only need to nullify V_{GS} because I_G (DC) is permanently zero. Similarly, for the substrate-source we only need to nullify V_{BS}.

Coverage of the proposed method would have been better fulfilled if we could investigate our claim for all three kinds of devices and in comparison with other techniques normally used. However, due to lack of space here we only present one example of a BJT amplifier.

Example

Example 2 – A BJT Feedback Amplifier: We are considering a two stage npn – pnp amplifier with feedback for this example, as shown in Fig. 7(a). We assume three DC sources that bias this amplifier, i.e., V_{CC} = 10V, V_{EE} = 10V, and V_{BB} = 1.1V. In normal situation the transistors are biased through these three supplies and the source v_s represents the input signal to the amplifier. The output waveforms are shown in Fig. 7(b).

To employ our proposed methodology we first adopt an arbitrary supply sequencing. We choose to apply the sources in three steps as: i) V_{CC} = 10V and the rest zero, ii) V_{EE} = 10V and the rest zero, and iii) V_{BB} = 1.1V and the rest zero. Evidently, we always nullify the ports before proceeding to the nest step. This process causes the v-i coordinates to move until the origin meets the Q-point for each port and in each step. This process continues and at the end the actual Q-points reside on the origins when the local biasing of the ports are completed. Table 1 shows the values for the augmenting sources in all four ports and for the three steps of local biasing. The final column is the sum of the three columns (additivity) and it shows the total values needed to locally bias the corresponding ports. Obviously, this is just one choice of supply sequencing adopted; other grouping and sequencing will end up with the same final result, but possibly with different path and convergence speed. Figs. 8(a) and (b) show the transistors being locally biased, and Fig. 9(a) shows the amplifier when the transistors are replaced by the local biased equivalents. Finally, Fig. 9(b) shows the response of the amplifier to the AC source v_s when the ports are locally biased

In comparing the simulated results of the original amplifier [Fig. 7(b)] with those of the amplifier with locally biased ports [Fig. 9(b)] we notice the differences in *DC* levels. In Fig. 7(b) both *DC* and *AC* signals are present, while in the case of locally biased all node voltages and element currents in the amplifier carry the *AC* signals, only. This indicates that in case of locally biased devices there is no need for coupling capacitances to block the DC.

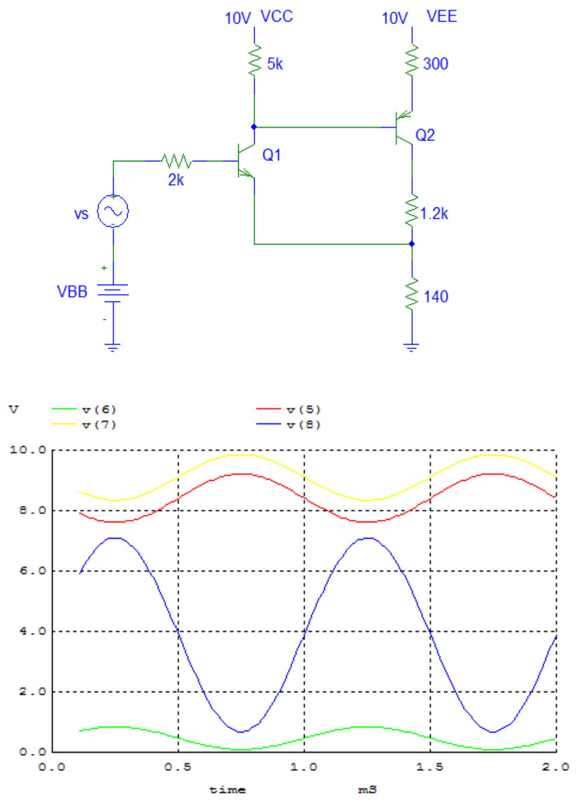

Figure. 7 - A two stage feedback amplifier, and its output responses.

Table 1 – The BJTs local biasing in multiple supply steps.

Sequence of Sources	V_{CC}	V_{EE}	V_{BB}	All Sources
V_{BE1}	-1.23e-08	-1.54e-09	6.30e-01	6.30e-01
V_{CE1}	1.00e+01	3.87e-09	-2.06e+00	7.94e+00
I_{B1}	1.64e-12	-5.49e-19	-3.45e-06	-3.45e-06
I_{C1}	-1.30e-11	1.78e-15	-4.23e-04	-4.23e-04
V_{EB2}	-1.00e+01	1.00e+01	7.05e-01	7.05e-01
V_{EC2}	-1.35e-07	1.00e+01	-4.81e+00	5.19e+00
I_{B2}	1.01e-10	-1.08e-12	-1.03e-04	-1.03e-04
I_{C2}	-1.00e-10	-1.10e-11	-2.88e-03	-2.88e-03

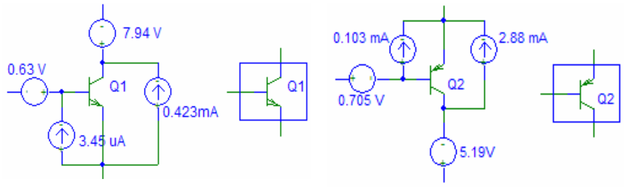

Figure. 8 – Local biasing of npn and pnp BJTs, with their symbols..

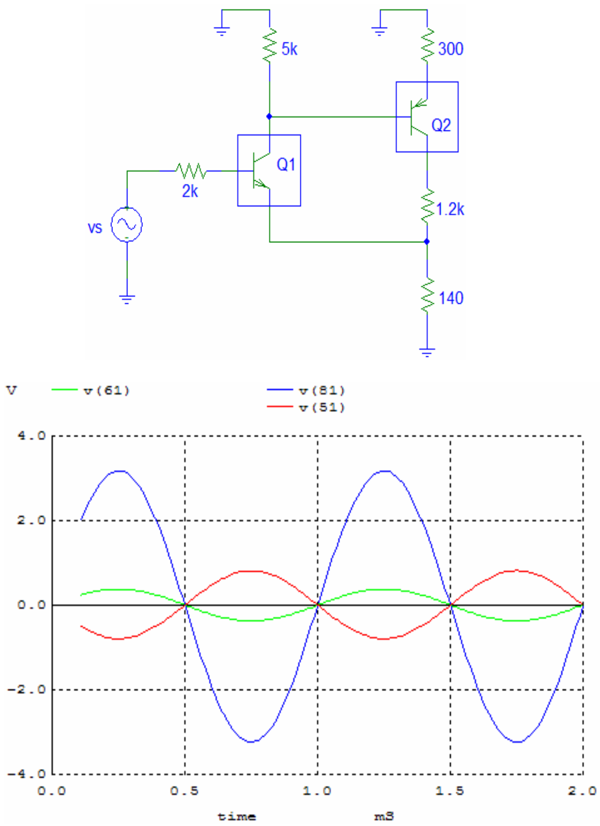

Figure. 9 - The feedback amplifier after the devices locally biased, and the output responses.

IV. Design Methodology

In the proposed methodology the design of an analog circuit needs to go through two stages of operations: *i)* linear stage, and *ii)* biasing stage. In the linear stage we can start from selecting the desired operating regions (OPs) for the nonlinear devices (diodes and transistors). This is a critical design step because it provide a complete freedom to select the OPs on the characteristic curves that could adequately respond to the design criteria, such as low signal distortion, high gain, sufficient voltage swing, low power loss and so on. In the second step the nonlinear devices are replaced with their small signal linear models. The resulting linear amplifier is then ready to go through the design procedure, where we have the option of selecting the right circuit topology and right component values, leaving the DC supplies completely out of the circuit. In this stage we can simulate and modify the linear circuit multiple times until we are satisfied with the results without being concerned about the biasing.

In the next stage we start locally biasing each nonlinear device by augmenting the ports by DC current and voltage sources, as described before. Our selection of augmented sources is simple and the sources are those that move the OPs to the desired locations on the characteristic curves, and selected in stage *i)*.

Theoretically the design procedure is completed at this point; however, the way the local biasing sources are spread throughout the amplifier may neither be desirable nor practical. At this point we enter into the third and the final stage of the design process, which is to replace the local biasing sources with fewer power supplies in the proper locations in the circuit. We notice that this step is also a linear step but a crucial one. The problem can simply be states as follows: *Replace the entire local biasing sources in the amplifier with fewer and properly located DC supplies so that the biasing of the nonlinear devices remain unchanged.* There are number of methods available to do this job, normally known as *source transformation*. One method is to use the superposition property and move the sources to proper locations one by one. The difficulty with this method is to formulate the process and to be able to do it through programming. Another technique is to use the method of large sensitivity to substitute the augmented sources by the actual power supplies [2]. This method is certainly more reliable and programmable. Other methods such as linear optimizations are other options for source allocation. In general, we must remember that in cases of large number of nonlinear devices and independently selecting the OPs reaching to a final few (one or two) supply sources may not be easy or even possible. In such cases compromising and accepting some tolerances may be necessary to provide us with a solution.

Algorithm 1 presents a step-wise procedure for the design of an analog circuit.

Algorithm 1:

1. For a selection of nonlinear devices (diodes and transistors) locate the desired operating regions (OPs) on the characteristic curves.
2. Locally bias each nonlinear device by augmenting its ports with DC current and voltage sources, such that the OPs move to the regions on the characteristic curves chosen in step 1.
3. Replace the nonlinear devices in the amplifier with their small signal linear models at the selected OPs.
4. Apply the design procedure to the linear amplifier circuit obtained. At this stage, choose the right circuit topology and the right component values, with no biasing (DC) supplies. Make changes until the criteria are met.
5. Include the sources used for local biasing of the devices into the linear amplifier circuit. Use source transformation methods to replace the DC (voltage and current) sources with the actual power supplies and in the designated locations.

V. Conclusion

With the complexity of today's analog circuit technology we need to remove or simplify the burden of handling nonlinearities in circuit biasing. A new methodology is presented in this article that provides a method of local biasing. The technique is based on a biasing that nullifies and isolates (not removed) nonlinear devices from the rest of the circuit, and eliminates them from the design process. This method allows the circuit designer to select the desired operational regions (OPs) on the characteristic curves of the nonlinear devices and start working on the rest of the (linear) circuit with no worry about the iterations or possible divergence.

VI. References

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