

Analog Circuit Design with Linearized DC Biasing

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Abstract— A new methodology is presented for the design of analog ICs. The method is based on a locally-biasing technique that DC-nullifies the ports. This entirely removes the general biasing of the circuit and applies it on each nonlinear device individually. The method isolates the nonlinear devices from the rest of the circuit, and excludes them from the design procedure. It allows the circuit designer to select the optimal operating regions for the devices, and then start working on the rest of the (linear) circuit with no need to perform nonlinear iterations or to worry about a possible divergence. An example of an operational amplifier design demonstrates the procedure.

I. INTRODUCTION

Analog and mixed signal integrated circuits technology has emerged as a dominant and powerful signal processing technology today. Particularly, with CMOS rapidly embracing the field in the past quarter of a century, analog circuit designs have become more challenging than ever. There is also major upgrading in the circuit criteria and performance such as low-voltage, low-power and high transistor counts that deserve new design techniques and methodologies. One such technique might be to allocate the operating points (OPs) of the nonlinear devices in regions that perform best for the design. In designing amplifiers, for example, we would like to place the OPs in locations on the characteristic curves that are almost linear with high gains. This is particularly important in the design of high gain and low power amplifiers, where multiple factors such as biasing, stage gains, impedance matching, bandwidth, noise, and distortion are main factors. The job becomes more complicated when the circuits with multi-stages and with positive feedbacks are involved, where the chances of getting unstable OPs are quite high. In some advanced circuit simulators, such as SPICE [3], methods based on Newton-Raphson iteration techniques are typically employed for allocating OPs. However, the major difficulties in these methods are the circuit convergence, and the numbers of iterations that are required to bring the OPs close enough to the desired regions.

Another problem in the area of analog circuit design is the lack of a reliable and systematic design methodology. There is no technique that can guide a designer from his/her criteria and design specifications to the final circuit without going through nonlinear analysis. In the case of an unskilled designer this may cost a lot in terms of time and efforts.

One difficulty arises from the fact that, usually, the circuit topology, including the supply (DC) sources and the nonlinear devices, are all bundled in one piece, pre-assigned to fixed locations in the circuit. In this situation when the entire circuit is simulated, with a poor selection of the initial conditions, the chance of getting a quick and smooth convergence is very slim [1-9]. Another problem is that the entire circuit is normally analyzed all together, as one piece. This is not particularly desirable in large and complex circuits, and it makes the convergence of the OPs very difficult. What is needed here is to break the circuit into parts with each part being specified through its ports. This procedure can be particularly helpful in the design, where tuning individual devices through their ports may lead to more desirable outcomes.

Our objective here is to establish a new methodology and employ techniques that help in designing highly complex analog circuits and to be able to access the desirable operating regions on nonlinear devices with minimum efforts. The method is based on a locally-biasing technique that DC-nullifies the ports. By applying this method the general biasing of the circuit is entirely removed, and instead biasing of individual devices is replaced. The method isolates the nonlinear devices from the rest of the circuit, and excludes them from the design procedure. It allows the circuit designer to select the optimal operating regions for the devices, and then start working on the rest of the (linear) circuit with no need to perform nonlinear iterations or to worry about a possible divergence. In other words, what is needed here is to anchor the nonlinear devices on their desired OPs first and then work on the entire (linear) circuit for the design, substituting the linear models for the locally-biased devices. It is shown that by employing local-biasing the nonlinear devices are totally DC-nullified (not removed) with respect to the rest of the circuit. As shown, this method

removes any difficulty related to iterations, instability and possible divergence.

The rest of the materials are arranged as follows. Section II of the paper discusses about preliminaries and properties used in this methodology. Section III covers the design procedure using the new technique. An algorithm puts the design procedure in a step-by-step process. An amplifier design is worked out in Section IV, and it is shown that the devices can be selected and put to work based on the design criteria with no need to go through a nonlinear iteration procedure. Finally we conclude the discussion in Section V.

II. PRELIMINARIES

The following definitions and assumptions are helpful in our discussions:

Definitions and assumptions: *i)* Networks are assumed to be memoryless and they can be linear or nonlinear, unless otherwise stated; *ii)* the term powerless refers to a network that has no internal source and no dependency to any external signal; *iii)* a null network refers to a network with no element; leaving the port nodes either open circuited or coalesced; *iv)* a port $j(v_j, i_j)$ with current i_j and voltage v_j , is said to be augmented by a current source I and a voltage source V if a current source I is added across the port, and a voltage source V is added in series with the port, as shown in Fig. 1. As a result, another port $k(v_k, i_k)$ is so created.

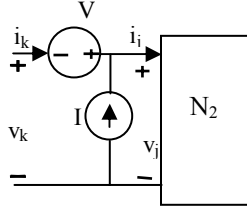


Figure 1. A port $j(v_j, i_j)$ of N_2 is augmented to create another port $k(v_k, i_k)$

Null Port: Consider a network N_2 connected to another network N_1 through a port $j(v_j, i_j)$. Port j is null if both i_j and v_j are zero.

Note that port j belongs to both N_1 and N_2 , but for N_1 it is specified as $j(v_j, -i_j)$. For brevity, the following properties are given without proof.

Property 1: In a network, if a port is null then a) the $i-v$ characteristic curve of the device looking from that port passes through the origin, and b) the origin is the device operating point.

Port nullification: Consider a network N_2 , connected to another network N_1 through m ports $j(v_j, i_j)$, for $j = 1, 2, \dots, m$. Port j is nullified if it is augmented, from both sides (N_1 and N_2), by current sources i_j and voltage sources v_j . Evidently, the result is the creation of m null ports $k(v_k, i_k)$, for $k = 1, 2, \dots, m$, as depicted in Fig.2

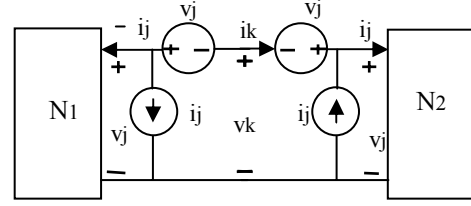


Figure 2. Port nullification procedure.

Property 2: Consider a network N_2 connected to another network N_1 , through one or more ports. If all the ports are nullified, removing all sources from N_1 (including any dependencies to external signals) has no effect on N_2 .

Notice in Property 2 that the network N_1 can become a null network, which leads to Property 3.

Property 3: Consider a network N_2 connected to another network N_1 , through one or more ports. If all the ports in N_2 are nullified, removing the entire network N_1 and leaving the null ports open circuit (or short circuit) would not affect N_2 .

Local-biasing: By definition, a port is locally-biased if it is nullified. Likewise, a network is locally-biased if all its ports are nullified.

It now becomes evident that connecting a locally-biased device (network) to a powerless network does not change the biasing condition of the device.

III. DESIGN OF AMPLIFIERS WITH SPECIFIED OPERATING POINTS

Properties 2 and 3, in section II, are two essential properties that help to simplify designing nonlinear analog circuits, such as amplifiers. In this method the design of an amplifier (or any other nonlinear circuit) needs to go through two stages of operations: *i)* the linear modeling stage, and *ii)* the linear biasing stage. In the linear stage we start by selecting the desired operating regions and OPs for the nonlinear devices (diodes and transistors). This step is crucial because the designer has complete freedom to select the OPs on the characteristic curves that could adequately respond to the design criteria. These criteria may include regions of maximum linearity; high gain, sufficient voltage swing and low biasing power loss. In the next step the nonlinear devices in the amplifier are replaced by their small signal linear models, and the circuit is ready to go through the design and simulation procedure. Here we have the choice of making any changes in the component values and even the circuit topology to meet the design criteria. We can simply design, simulate and modify the circuit multiple times until we are satisfied with the results without being concerned about the DC biasing.

We are now ready to locally-bias the transistors by augmenting the ports with DC voltage and current sources that push the OPs to the desired locations (as specifies earlier) and bring them to the origins. This is, in fact, the port nullification that was discussed in Section II. We recall from

Section II that when the devices are locally-biased (augmented) they can be connected to the rest of the amplifier circuit (the linear circuit with no supply source) and still maintain their biasing unaltered and, at the same time, leave the criteria in the amplifier circuit unchanged.

Theoretically the design procedure is completed at this point, except for having a distributed (local) biasing rather than a central and global biasing for the amplifier. Also notice that up to this point we have avoided doing any nonlinear DC analysis. However, the way the local-biasing has caused the DC supplies to be spread throughout the amplifier may neither be desirable nor practical, and we need to resolve it.

At this point we enter into the third and the final stage of the design process, which is to replace the locally-biased sources in the linear circuit with fewer power supplies in the circuit such that no change occurs in the OPs of the devices. This is an important step to tackle in the amplifier design, but the good news is that everything here is linear. There are a number of methods available that are capable to do the job. One method is to use the superposition property and move the sources to the designated destinations by source transformations. The difficulty with this method is how to formulate the process and do the programming. Another method is to again use the superposition along with large sensitivity analysis to substitute the augmented sources by the normal power supplies with specified values. This method is certainly more reliable and programmable. Other methods such as linear optimization are also viable options for source allocation. For brevity purposes we leave this topic for further researching.

In Algorithm 1 a step-wise procedure is presented that demonstrates the sequence of operations needed to design an amplifier, as proposed:

Algorithm 1:

1. Select the desired operating regions for the nonlinear devices (diodes and transistors) that are going to be used in the amplifier, and then DC locally-bias the devices.
2. Replace the locally-biased nonlinear devices in the amplifier by their small signal linear models at the selected operating regions, and design the amplifier for the best performances.
3. Get back and replace the linear model of each device by its original locally-biased nonlinear device.
4. Use a source transformation method to reduce the number of DC supplies in the amplifier (sources used for the local-biasing). This must ultimately result in one or two power supplies, typically needed for the biasing of an amplifier.

The method discussed so far can be implemented on any nonlinear circuit or device. If multiple numbers of nonlinear devices are used in a circuit we can handle the case in two different ways. One way is to take each nonlinear device as a separate entity and deal with its ports as a nonlinear network

connected to the rest of the network. The second way is to group all (or partial) nonlinear devices into one nonlinear network and handle them collectively. Although the later method has some merit over the first one but because of some complexity involved in the procedure we only consider the former case, i.e., we deal with nonlinear devices individually in this article.

Within the three major semiconductor components p-n junction diodes are one-port devices. Bipolar-junction transistors are generally considered two-ports, but they can be turned into two one-port devices if Ebers-Moll large signal model is used for the transistors [11]. MOS transistors are considered three-port devices but only four sources are needed to locally-bias the device. This is because for the drain-source we need both ID and VDS sources to nullify the port, but for the gate-source and the substrate-source we only need to use VGS, and VBS sources respectively to nullify the ports.

IV. IMPLEMENTATION AND EXAMPLE

We conclude the design procedure in this article by going through an example of a simple basic operational amplifier.

Example – A Three-stage CMOS Op-Amp: For this example we are going to design a simple three-stage operational amplifier without stability feedback and with configuration given in Fig. 3. Note that for simplicity the current mirrors are substituted with the equivalent current sources, and also the substrate connections are omitted from the figure.

To proceed with this design we initially select the DC operating regions for the transistors. These regions include the values of V_{ds} , V_{gs} , V_{sb} , and I_d for individual transistors. However, for I_d we also need to know the W/L ratio of the transistors. To solve the problem we first assign nominal values for W/L and simulate each individual transistor with the assigned values (V_{ds} , V_{gs} , V_{sb} , and W/L) to find I_d . Since I_d and W/L are linearly dependent we can then adjust W/L ratio to achieve the right I_d for the design. Other design parameters such as the resistor values, supply voltages and currents are not specified and can be obtained in the following linear circuit design procedures. Figure 4 shows the result of applying the first step in Algorithm 1, where the transistors are augmented by current and voltage sources to perform locally-biasing in the amplifier. The models for both nMOS and pMOS transistors are depicted with their symbolic representations.

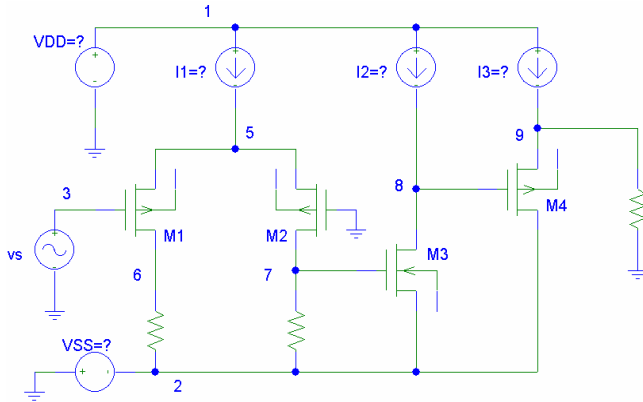


Figure 3. A selected configuration for a three stage operational amplifier

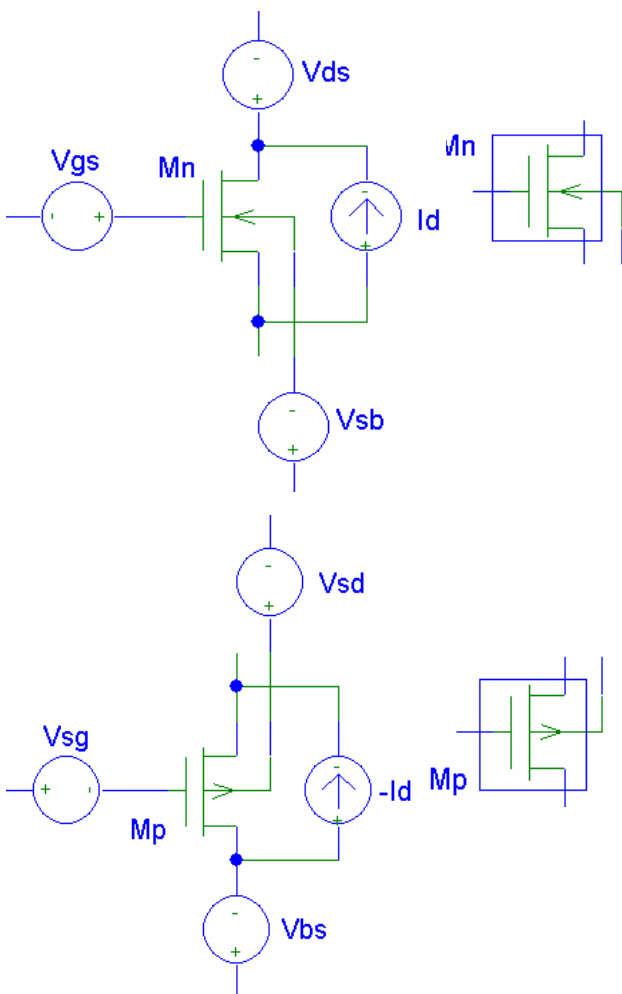


Figure 4. Two augmented (locally-biased) models of nMOS and pMOS with their symbolic representations

Table I shows the selected voltages and currents for all four transistors used in this amplifier. Before we proceed further there are several important points to note: The V_{ds} for all transistors are selected such that the voltage swing could be maximized close to 6 volts, particularly for the buffer stage (M_4). Another observation to be made is the selection of the current gain for the buffer stage which is about 16.5 times, while there is hardly any current gained from differential stage to the (voltage) gain stage. Also notice that V_{gs} is the largest for the buffer stage and that is to generate larger current for the output. Finally, the selections of V_{sb} are carefully done to adjust to the operating points.

TABLE I. THE DESIGN VALUES FOR THE LOCAL-BIASINGS

Augmented Sources	V_{ds}	V_{gs}	V_{sb}	I_d
pMOS-1	-5.55	-1.65	-3.35	-2.16e-05
pMOS-2	-5.55	-1.65	-3.35	-2.16e-05
nMOS-3	2.98	1.10	0.00	6.85e-05
pMOS-4	-4.92	-1.97	-5.05	-1.12e-03

Selection of the biasing currents and voltages of the transistors helps to select the size of the transistors, as mentioned earlier. For this particular design the transistors lengths are assigned all $L = 2 \mu\text{m}$ and the transistors widths, according to the locally-biased values, are selected as:

$$W_1 = 15 \mu\text{m}, W_2 = 15 \mu\text{m}, W_3 = 30 \mu\text{m}, W_4 = 500 \mu\text{m}$$

Similarly the resistance values are accordingly obtained as $R_{M1} = 51\text{K}$, $R_{M2} = 51\text{K}$, and $R_{M4} = 4.5\text{K}$. Next we need to replace the transistors by their linear small signal models and calculate the gains, bandwidth, and other design specifications. The simulation program WinSPICE is used for the analysis of the linear model of the amplifier.

After the basic design is over and all linear components are assigned we need to replace the linear models of the transistors with their corresponding counter parts. Figure 5 shows the amplifier configuration with the locally-biased transistors replaced for their linear models. Notice that no external supply sources are needed to run the circuit at this stage. Only v_s as the input signal source is sufficient to do the transient analysis. The amplifier is simulated and the results are verified. Fig. 6 shows both the transient response and the frequency response of the amplifier. Note that all node signals in the transient response lack any DC component, which is due to local-biasing of non-linear devices.

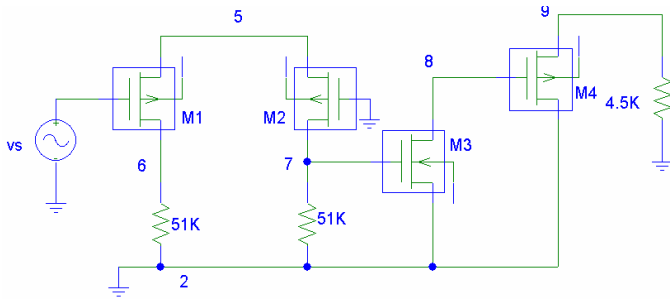
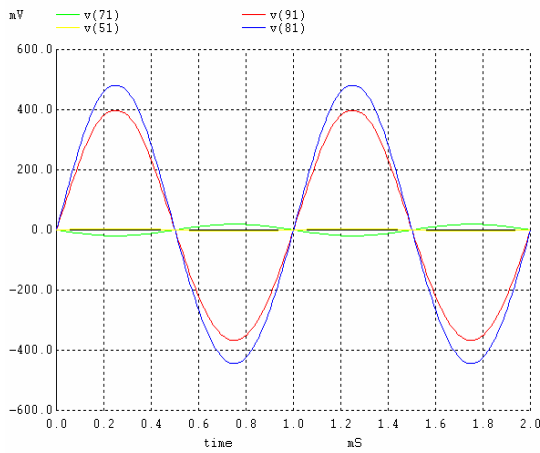
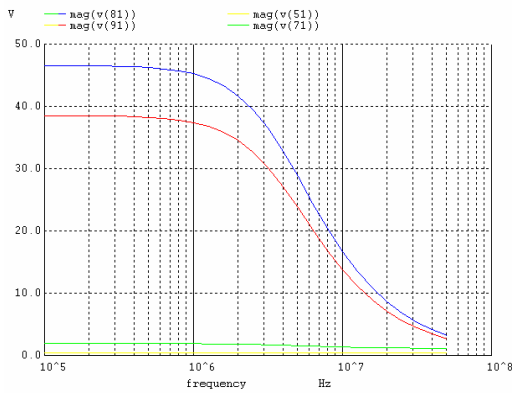


Figure 5. The Op-Amp configuration with locally-biased devices



(a)



(b)

Figure 6. The transient and frequency responses of the Op-Amp with locally-biased configuration.

In employing the final step of Algorithm 1 we need to substitute for the local-biasing sources by assigning external sources in the designated locations in the amplifier. This is done by a source transformation procedure. The procedure (not explained here) results in three current sources $I_1 = 43$

μA , $I_2 = 68 \mu\text{A}$, and $I_3 = 1.12 \text{ mA}$ for the global biasing, and also addition of two voltage sources $V_{DD} = 5 \text{ V}$ and $V_{SS} = 5 \text{ V}$ for the voltage swings.

V. CONCLUSION

With the complexity of today's analog circuit technology we need to remove or simplify the burden of handling nonlinearity in circuit biasing. A new technique is presented in this article that does exactly this. The technique is based on local biasing of nonlinear devices that nullifies and isolates (not removed) the devices from the rest of the circuit, and eliminates them from the process of design. This method allows the circuit designer to select the desired operational regions on the characteristic curves and start working on the rest of the (linear) circuit with no worry about the divergence. An example of an operational amplifier design demonstrates the procedure. The results of the example show the simplicity and accuracy of the technique used.

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