

A New Methodology to Simulate Circuits with Nonlinear Devices

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Abstract— In this presentation we are offering a new approach to handling circuits with nonlinear devices. Instead of regular biasing this method presents a way to localize the biasing by using “port nullification”. The method is built around the concept of additivity, a property of superposition that has been widely used in linear circuits. This method allows the circuit designer to select a scheme of applying dc (or ac) sources in multiple steps to better control the dc operation of the circuit and get faster convergence. The method is tested through some examples and by using SPICE simulator.

I. INTRODUCTION

Finding operating points for circuits that carry nonlinear devices have always been difficult, and time consuming. The process may even become unsuccessful if the circuit is complex or multiple operating points are involved [1 - 8]. In some advanced circuit simulators, such as SPICE [9], methods based on Newton-Raphson iteration techniques are typically employed. But the major difficulties in these methods are circuit convergence, and the number of iterations that is required to get close enough to the desired operating points. The problem usually arises from applying the entire dc sources at once and with a poor selection of the initial conditions for the operating points. Large and unregulated steps in search for operating points increase the chances of going out of range, and ultimately ending with non-convergence.

We present a new procedure in this article that allows controlling the search for final operating points through gradually applying the supply sources and in a manner that helps quick convergence. This will give a nonlinear circuit designer to group and prioritize the application of the dc sources such that with a selective regime the circuit operation gradually moves to its final destination. It is interesting to note that the method works with almost any memoryless nonlinear device and in case of multiple operating points one is able to converge on any specified operating point by choosing a specified pattern of *supply sequencing*. The key concept that makes all this possible is recording (storing) the partial operating points that are found in each step of the operation, and use them as the starting points (the origins of the $v - i$ coordinates) for the

next step. This procedure continues until all sources are used and the final operating points are found. This method is called *Port Nullification*, and it works as follows:

Section II discusses about port nullification in one-port as well as multiple port nonlinear circuits. In Section III we deal with implementation of the methodology. Two examples are worked out in this section, one for one-port nonlinear devices and the second example is given for multiple port nonlinear cases.

II. PORT NULLIFICATION

For simplicity let us assume a circuit N having a single nonlinear two-terminal device D. Let us make a selection of partial dc sources and apply them to N. With this selection of supplies the operating point of the device moves to a point Q_1 , on the characteristic curve, represented by the current I_1 and the voltage V_1 on the port. Now, the whole idea is to keep the operating point Q_1 unaltered while we remove the dc sources. Obviously if we just remove the supply sources in the circuit both I_1 and V_1 become zero, and Q_1 merges into the origin. To prevent this we can augment the device with two current and voltage sources to keep the device running and unaffected while the supplies are removed from the circuit N. The augmentation is applied by adding a current source (memory) I_M connected in parallel with D, and a voltage source (memory) V_M connected in series with D. Primarily, both I_M and V_M carry zero values when we start the simulation, but as the operating point Q moves on the device characteristic I_M and V_M pick up the changes (I_1 and V_1) and store the last values, after the supplies are removed. As a result, the augmented device always shows zero current and zero voltage from the outside when the device is actually running at its normal operating point Q_1 (I_1 and V_1), but no supply is present in the circuit N. Now, when the first set of supplies are removed and the second set of selected supplies are applied to the circuit the device operating point moves again, and goes from Q_1 (now the origin) to a new place Q_2 , with new port current and voltage I_2 and V_2 , respectively. Similarly, when the second set of supplies are removed from the

circuit the new values in I_M and V_M keep running D at its operating point Q2, but the port current and voltage of the augmented device looking from the outside are again back to zero, or simply, the origin has moved to the operating point Q2. Now, to see how the additivity is working here, we realize that the stored augmented values in the sources I_M and V_M are now changed to $I_M = I_1 + I_2$, and $V_M = V_1 + V_2$, which is a proof for additivity. We can continue applying other sets of supply voltages one at a time and accumulate the augmented memory values in I_M and V_M such that

$$I_M = \sum_{j=1}^n I_j, \text{ and } V_M = \sum_{j=1}^n V_j$$

Where I_j and V_j represent the j th step move of the Q point from the origin and n is the total number of supply groups in the circuit, applied one at a time.

A similar procedure follows for circuits with multiple nonlinear devices, and also devices with multiple ports. For instance, a two port nonlinear device is augmented at both ports, and the operating point in each port is stored at its own augmented current and voltage sources.

In our presentation, the *Port Nullification* methodology is applied to circuits containing p-n junction diodes, bipolar transistors, and MOS transistors. It is interesting to note that with substrate-source counted as a port in MOS transistors the device is characterized by three ports, but only four sources are used in the augmentation, i.e., I_D , V_{DS} , V_{GS} , and V_{BS} . What it means is that, in applying the sequences of supplies to a circuit with MOS devices we need to keep four variables, I_D , V_{DS} , V_{GS} , and V_{BS} , for each device before we discard the supplies from the circuit. And with these sources updated (accumulated) each time each time that a set of supplies are used the circuit will finally ends up with no supply being present, but instead the ports of the nonlinear devices are augmented and nullified. This circuit is now ready to get the actual input signal applied, and the output signals are definitely free from the supply (dc) signals.

Port nullification is certainly an analysis and simulation tool at the present time, but it can be developed to play a major role in the design of the analog circuits as well.

Several examples including some feedback amplifier are carried out using the *Port Nullification* methodology. The results show quite significant improvements in convergence and much lower number of iterations needed to converge compared to the ordinary methods. The variety of choices of *supply sequencing* makes it a valuable tool for a professional analog circuit designer to efficiently work with complex cases.

III. IMPLEMENTATION OF THE METHODOLOGY

We start the implementation of the Nullification methodology by a simple example of an MOS transistor circuit with one port only. Later we expand the application to multiple nonlinear port circuits. In the second example we pick up a double bipolar transistor feedback amplifier for our analysis.

A. Example 1

Consider the circuit of Fig. 1(a), where two parts of a circuit are connected through a Port j (v_j , i_j). Suppose the MOS diode M1 is characterized by $i = K(v-1)^2$ mA, for $v > 1V$, where $K = 0.5$ mA/V². The analysis shows that Port j is not definitely a null port, since $I_j = 1$ mA and $V_j = 3$ V. Next, we augment Port j by current and voltage sources I_j and V_j , from both sides, to create Port k (v_k , i_k), as shown in Fig. 1(b). Now, Port k becomes null since both I_k and V_k are zero. Note that, although the $i-v$ characteristic curve for Port j does not pass through the origin but that of Port k does. It is important to note that Port k is also a port of circuit N_1 , on the left hand side, and hence its characteristic curve must pass through the origin as well. This simply means that, the (Thevenin or Norton) equivalent circuit of N_1 , looking from Port k , can only be resistive with no source inside, i.e., we can remove all sources from N_1 with no effect on N_2 , as shown in Fig. 1(c). This leads to the following property.

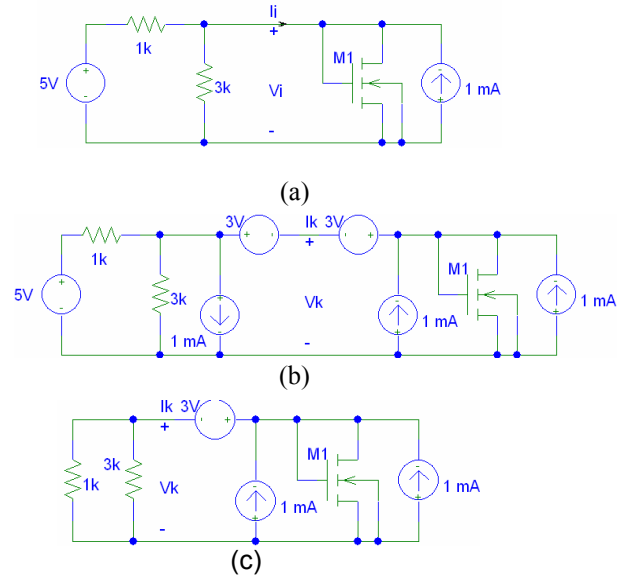


Fig. 1 – (a) two circuits N_1 and N_2 separated by Port j , (b) creation of null Port k , (c) simplified null Port k

Property 1: Consider a circuit N_2 connected to another circuit N_1 through a single Port j . If Port j is null then all sources in N_1 can be removed without affecting N_2 .

The proof of Property 1 is evident, because the only source of power to N_1 can be through Port j . But being a null port, Port j cannot transfer any signal (v or i) from N_2 to

N_1 . Hence, all currents and voltages in N_1 remain zero, and cannot influence N_2 . The converse, however, is not necessarily true, i.e., N_1 can have sources while Port j is still a null port, as we notice in Example 1.

Another point to consider is that, when a port is nullified it must be nullified from both sides [Fig. 1(b)]. On the other hand, an obvious choice of nullification of a port, according to Property 1, is to remove all sources from that portion of the circuit that the port represents. What it means is that, if two circuits (linear or nonlinear) N_1 and N_2 are connected through a single port, one way to remove the supply sources from N_1 and keep N_2 still running unaltered is to nullify its port. Similarly, in order to keep the operating point(s) of a nonlinear device fixed on a certain location(s) on the characteristic curve(s) is to run the device by the biasing supplies, nullify the port(s) and then remove the supplies from the circuit.

The method discussed so far can be implemented on any nonlinear circuit or device. If, however, multiple numbers of nonlinear devices are used in a circuit we can handle the case in two different ways. One method is to take each nonlinear device as a separate entity and deal with it as a nonlinear network. The second method is to group all (or partial) nonlinear devices into one nonlinear network and handle them collectively. Although the later method shows some merit, but because of some complexity involved in the procedure we only consider the former case, i.e., we deal with nonlinear devices individually in this article.

Within the three major semiconductor components, diodes, BJT and MOS, p-n junction diodes are one-port devices and the rest are multiple-port. BJTs are typically two-port devices, but they can be turned into two one-port devices if *Ebers-Moll* large signal models are used [11]. MOS transistors, on the other hand, are considered three port device but only four sources are needed for port nullification. For the drain-source port we need to nullify I_D and V_{DS} , for the gate-source we need to nullify V_{GS} , and for the substrate-source we need to nullify V_{BS} to inactivate the entire MOS device.

B. Example 2 – A BJT Feedback Amplifier:

For this example we take a two stage npn – pnp amplifier with feedback, as shown in Fig. 2(a). We consider three dc sources for this amplifier, $V_{CC} = 10V$, $V_{EE} = 10V$, and $V_{BB} = 1.1V$. In normal situation the transistors are biased and the input signal v_s will generate the output signals in the amplifier, as depicted in Fig. 2(b). Next, we adopt a supply sequence in three steps as: i) $V_{CC} = 10V$, ii) $V_{EE} = 10V$, and iii) $V_{BB} = 1.1V$, and nullifying the ports, after each step. Table 1 show the supply sequencing applied in this example. Also the augmented source values for each step are shown in this table. Evidently, this is only one choice of supply sequencing, other grouping of supplies and

the sequence of applying them to the amplifier could be adopted, which all eventually end up with the same results. But the difference may be in the number of steps required for convergence. Figs. 3(a) and (b) show the transistors being inactivated at the last step in the procedure, and Fig. 4(a) indicates the amplifier when it is exhausted of all its dc sources, and the transistors are replaced by the equivalents with nullified ports. Finally, Fig. 4(b) shows the response of the amplifier to the ac source v_s .

Before we leave this example we need to discuss several important points:

- When we compare the simulated results from the original amplifier, Fig. 2(b), with those from the amplifier with nullified ports, Fig. 4(b), we notice their differences in dc levels. In Fig. 2(b) both dc and ac signals are present at the outputs and for the removal of the dc from the output we normally need to use coupling capacitances. While in the case of nullified ports all node voltages and element currents in the amplifier carry only the ac signal.
- In Table 1 we notice that the last column, representing the sum of all supplies, is the algebraic sum of the other three columns, each representing one of the supplies. This is the *additivity* property, presented in this methodology.

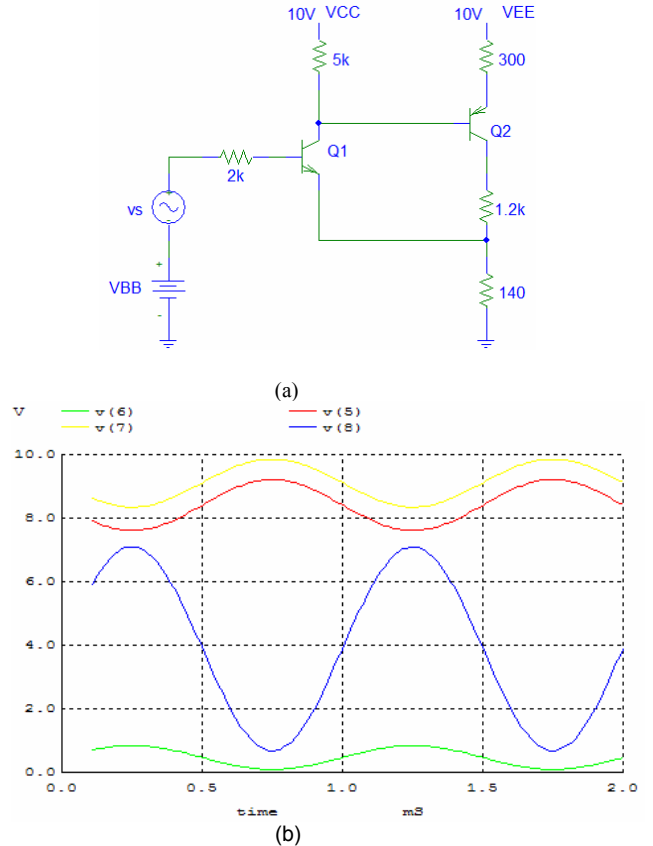


Fig.2 (a) - A two stage feedback amplifier, (b) The output responses

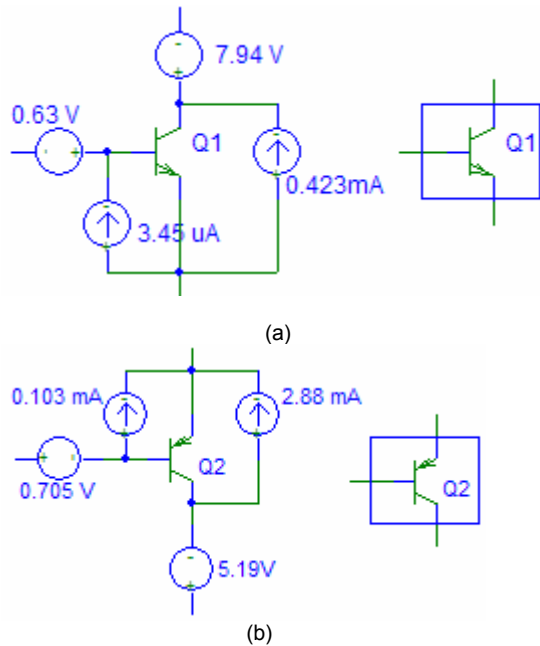


Fig. 3 – Inactivation of the BJTs, (a) the npn, and (b) The pnp

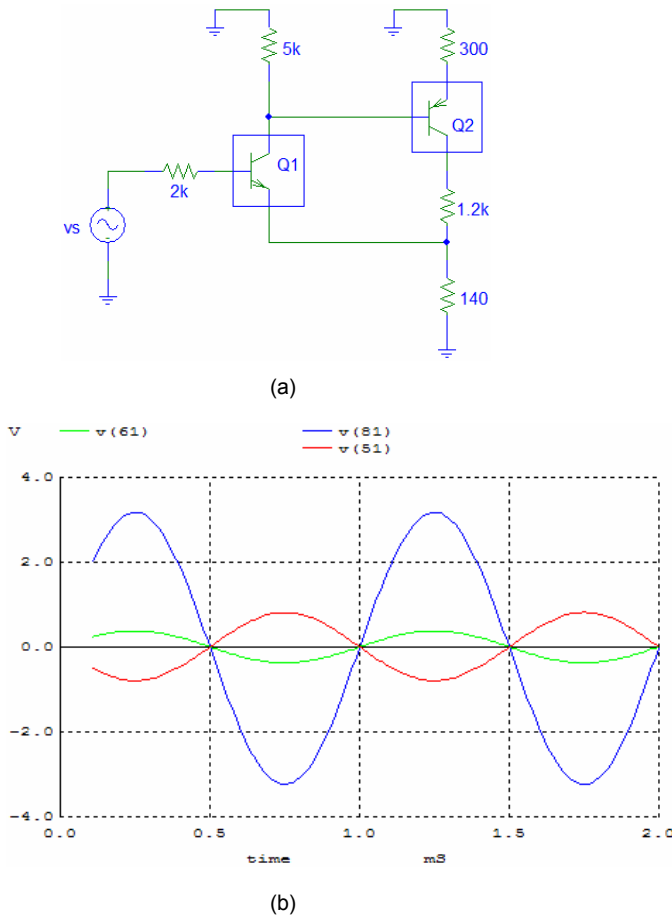


Fig. 4(a) - The feedback amplifier after the devices' inactivation, and (b) the output responses

TABLE I

THE BJTS INACTIVATION RESULTS IN SUPPLY SEQUENCING

Sequence of Sources	V_{CC}	V_{EE}	V_{BB}	All Sources
V_{BE1}	-1.23e-08	-1.54e-09	6.30e-01	6.30e-01
V_{CE1}	1.00e+01	3.87e-09	-	7.94e+00
I_{B1}	1.64e-12	-5.49e-19	-3.45e-06	-3.45e-06
I_{C1}	-1.30e-11	1.78e-15	-4.23e-04	-4.23e-04
V_{EB2}	-	1.00e+01	7.05e-01	7.05e-01
V_{EC2}	-1.35e-07	1.00e+01	-	5.19e+00
I_{B2}	1.01e-10	-1.08e-12	-1.03e-04	-1.03e-04
I_{C2}	-1.00e-10	-1.10e-11	-2.88e-03	-2.88e-03

REFERENCES

- [1] C.W. Ho, A.E. Ruehli, and P.A. Brennan, "The modified nodal approach to network analysis," *IEEE Trans. Circuits Syst.*, vol. CAS-22, no. 6, pp. 504-509, June 1975.
- [2] C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*. New York: McGraw Hill, 1969.
- [3] Y. Inouea, "Dc analysis of nonlinear circuits using solution-tracing circuits," *Trans. IEICE (A)*, vol. J74 A, pp. 1647-1655, 1991.
- [4] ____, "A practical algorithm for dc operating-point analysis of large scale circuits," *Trans. IEICE (A)*, vol. J77-A, pp. 388-398, 1994.
- [5] M. M. Green and A. N. Willson Jr., "How to identify unstable dc OPs," *IEEE Trans. Circuits Syst. I*, vol. 39, pp. 820-832, Oct. 1992.
- [6] ____, "An algorithm for identifying unstable OPs using SPICE," *IEEE Trans. Computer-Aided Design Integrated Circuits*, vol. 14, pp. 360-370, Mar. 1995.
- [7] M. M. Green, "The augmentation principle of nonlinear circuits and its application to continuation methods," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 45, no. 9, pp. 1002-1006, Sept. 1998.
- [8] R. C. Melville, L. Trajkovic, S.C. Fang, and L. T. Watson, "Artificial parameter homotopy methods for the dc OP problem," *IEEE Trans. Computer-Aided Design*, vol. 12, no. 6, pp. 861-877, Jun. 1993.
- [9] L.W. Nagel, "SPICE2, A computer program to simulate semiconductor circuits," Univ. of California, Berkeley, CA, Memorandum no. ERL-M520, 1975..
- [10] B. P. Lathi, *Linear Systems and Signals*. New York: Oxford University Press, 2005.
- [11] A. S. Sedra, and K. C. Smith, *Microelectronic Circuits*. New York: Oxford University Press, 2004.