

Use of Conditional Additivity in Circuits with Exponential Nonlinearities

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Abstract—A new methodology is proposed for analysis and simulation of circuits with exponential nonlinearities. It is shown that the additivity, a property of superposition, works here provided that the devices are conditioned after each application of supply sources. The methodology is used for circuits with p-n junction diodes, and it is extendable to include bipolar transistors when the devices are replaced by their Ebers-Moll models. As an example a diode circuit is fully discussed and the SPICE simulation results are discussed.

I. INTRODUCTION

Finding the dc operating points (OPs) of nonlinear devices in a circuit is important for the design of analog circuits. However, the job becomes difficult and often complicated for sizable circuits, particularly those with positive feedbacks, where the chance for the OP being unstable is quite high. In some advanced circuit simulators, such as SPICE [1], methods based on Newton-Raphson iteration techniques are typically employed. But the major difficulties in these methods are circuit convergence, and the number of iterations that is required to get close enough to the desired OPs. The problem usually arises from applying the entire dc sources at once and with a poor selection of the initial conditions for the OPs. Large and unregulated steps in search for OPs increase the chances of going out of the range, and ultimately ending with non-convergence [2 - 8].

For linear circuits the situation is different. When a system is considered to be linear the superposition principle can be applied. This is why the techniques of linear circuit and system analysis have been so well developed. Analysis of linear circuits is relatively simple and straight forward; the responses are accurate and the convergence is fast. Superposition, in a memoryless circuit, consists of two properties, *additivity* and *homogeneity*. The additivity property states that, if several inputs are acting on a system, then the total effect on the system due to all these inputs can be determined by considering one input at a time while assuming all the other inputs to be zero [9,10].

By definition, a system is nonlinear if superposition does not hold [9]. Hence, we cannot expect to formally apply either additivity or homogeneity to nonlinear circuits. However, while homogeneity is far from being used in

nonlinear circuits, but the additivity property is, provided that the circuit is *conditioned* after the application of each individual or group of supply sources. To be more specific, we are going to show that additivity applies if the operating point (OP) in each and every nonlinear component in the circuit is adjusted after the application of each individual or group of supply sources. But, what is this conditioning and adjustments and how does it work?

In practice, we normally handle nonlinear circuits, such as amplifiers, by first biasing the circuit and then applying the ac signal, which indeed is another way of conditioning, and a form of additivity (dc plus ac) works here. The biasing is to condition the amplifier circuit such that the operating points of the nonlinear devices move to reasonably linear portion on the characteristics, and while the dc supplies are kept in the circuit the ac signal is applied. To show that the additivity property works here we can verify any response (current in a circuit component or voltage of a node) in the circuit. For instance, the output voltage v_o in the circuit is the sum of two components V_o , which is generated because of the biasing, and v_o that is due to the ac signal. Now, if we remove the biasing supplies and apply only the ac signal, we also get only a more distorted v_o , and not the one with the biasing. Although this biasing helps to move the operating points to desired locations on the characteristics and to benefit from the limited linearity in the design, but biasing itself may pose some difficulties. The circuit may end up with non-convergence situation or unsatisfactory operating points, as we discussed earlier. The other serious problem with biasing is how to discard the dc signal from entering into the input and the output components. Coupling and by-pass capacitors are typically used in regular amplifier designs to stop the dc. These capacitors are often bulky and cut the amplifier bandwidth. In cases of analog integrated circuits, such as operational amplifiers and OTAs, careful use of symmetry and certain dc balancing may serve to remove the biasing effect on the output. But still the need for some final voltage adjustments may cause problems.

What we propose here is to localize the biasing in the analysis and simulation of analog circuits with exponential nonlinearities. The point is that, instead of jumping to certain operating points on the characteristic curves, through

the external supply sources, condition the devices themselves such that the OP falls into the origin and free from biasing. In this situation the ac signal is the only signal present in the can circuit. This makes our main concept in this presentation, as we discuss it later.

In section II we introduce the operating point adjustments for p-n junction diodes. It is shown that the additivity, a property of superposition, works for devices with exponential nonlinearities provided that the devices are conditioned after each application of supply sources. The methodology is further developed in Section III by using SPICE simulation. A diode circuit is given as an example.

II. OPERATING POINT ADJUSTMENT

Let us consider the circuit shown in Fig. 1(a) attached to a nonlinear device D. Here, the biasing has moved the operating point on the device characteristic to Q. But if we remove the supply sources inside the network N the operating point falls to the origin O, the hard nonlinear portion of the characteristic curve [Fig. 1(b)]. Our proposed solution is to remove the dc supplies from the network N, and instead condition the device D to have the i-v coordinates moved to point Q, as shown in Fig. 1(c).

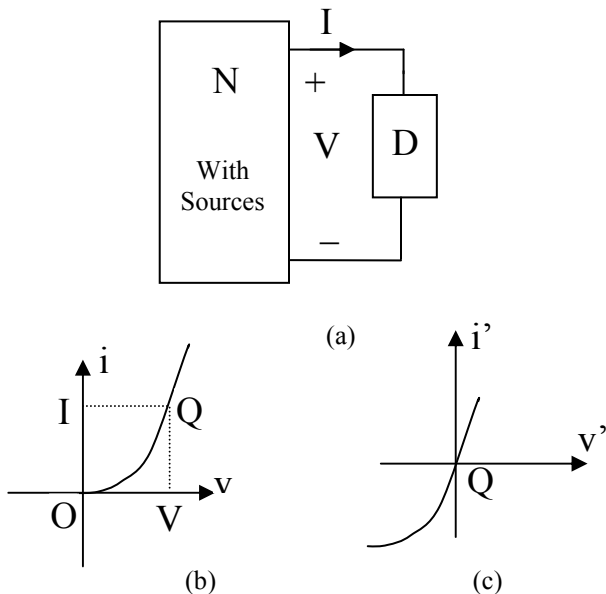


Fig. 1 – (a) Circuit with a nonlinear device D, (b) The device characteristic, and (c) The device characteristic after being conditioned.

Now, we need to specify how the conditioning can cause such a change in the circuit performance. We are going to show that for certain nonlinearities, such as exponential functions, one way to do the conditioning is to reassign new values to some functional parameters. For instance, we will show that by changing the reverse-biased saturation current I_s in the p-n junction characteristic

equation we will be able to move the origin to any location on the characteristic curve.

The second and a very important objective in our proposed method is to apply the additivity property to circuits with exponential nonlinearities. Here we show how in a nonlinear circuit we can approach to the desired operating points by a step by step procedure of applies the dc sources. The additivity property works here as it does in linear circuits, except that we need to adjust some functional parameters. The key concept here is to *condition* the devices after each biasing. We introduce the methodology through the following theorem.

Theorem 1: Consider a p-n junction diode D with the current i and the voltage v , as shown in Fig. 2(a), and characterized by Eq. (1). Suppose the diode is operating at an OP Q with a current I and a voltage V [Fig. 2(b)]. We can achieve moving the i-v coordinates to a new place, such that the origin is located on the operating point Q, as shown in Fig. 2(c), by replacing the reversed-biased saturation current I_s with $I_s' = I + I_s$.

$$i = I_s (e^{v/nV_T} - 1) \quad (1)$$

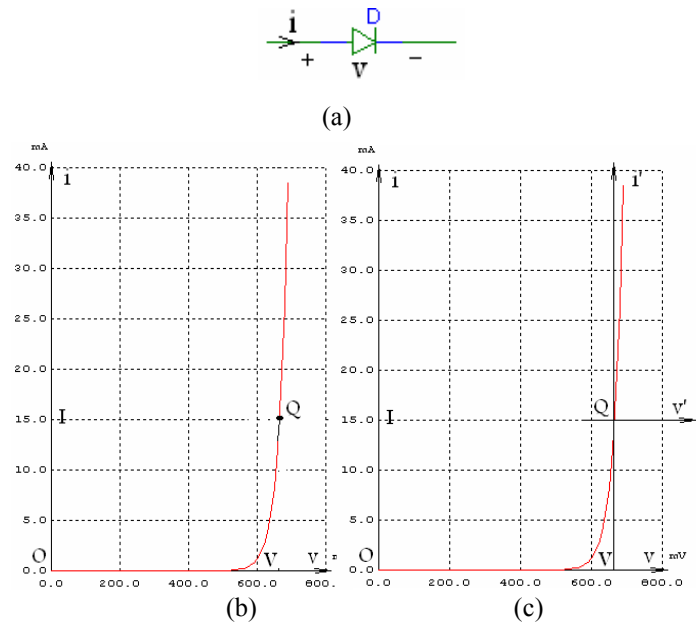


Fig. 2 – (a) a diode D, (b) the diode i – v characteristic with an operating point Q specified, and (c) the new coordinates after I_s is adjustment.

To prove Theorem 1, we first assume an operating point Q on the characteristic curve, with current I and voltage V , as indicated in Fig.2(b). Next we adopt a new i' - v' coordinates by moving the axis to the point Q on the characteristic curve, as shown in Fig.2(c). Now to modify Eq. (1) we need to do the followings:

$$v = v' + V, \text{ and } i = i' + I \quad (2)$$

We also have

$$I = I_s(e^{V/nV_T} - 1) \quad (3)$$

After substitution from Eq. (2) into Eq. (1) and taking Eq.(3) into consideration we get

$$i' + I = I_s(e^{v'/nV_T} - 1) \quad (4)$$

Or simply

$$i' = I_s(e^{v'/nV_T} - 1) - I_s(e^{V/nV_T} - 1) = I_s e^{v'/nV_T} (e^{V/nV_T} - 1) \quad (5)$$

With more simplification we get

$$i' = (I + I_s)(e^{v'/nV_T} - 1) = I_s'(e^{v'/nV_T} - 1) \quad (6)$$

This proves the theorem.

Although the theorem is true for all cases of I_s' , but to achieve a quick convergence it is recommended that for negative current I , i.e. $I_s' \ll I_s$, we use the voltage rather than the current variable to adjust the i - v coordinates. To do this we can write

$$I_s' = I_s e^{V/nV_T}, \text{ or } V = nV_T \ln(I/I_s + 1) \quad (7)$$

Now to avoid the reverse biased voltage run-off we can augment a voltage source V in series with the diode and form a new symbol D_1 , as shown in Fig. 3.

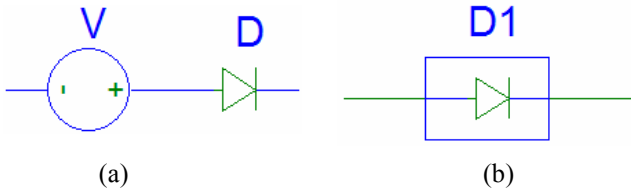


Fig. 3 – (a) Augmented diode D with a voltage source V , and (b) the equivalent symbol D_1 .

Notice that for the reverse biased diode the voltage V is negative, and this helps to stop the reverse biased voltage run off, and thus quicker convergence. To verify, suppose the diode D is off with the reversed biased voltage $V_D < 0$. Now, if we assign V close enough to V_D then a new diode D_1 [Fig. 3(b)] will emerge which operates about the origin, and hence much easier to handle.

III. SPICE ASSISTED ANALYSIS

To verify the proposed methodology we are going to run examples with p-n junction diodes. The method can certainly be extended to include bipolar transistor circuits.

This is because, in modeling the devices we can always replace a transistor by its Ebers-Moll model, which originally consists of two diodes and two dependent current sources. However, due to lack of space in this presentation we cover only one example of diode circuits.

As a popular and well developed analog simulator we use SPICE (WinSpice) for our example. However, because SPICE does not leave much room for the user to manipulate the model set ups, we need to impose some external settings before we proceed into running the example. For instance, to avoid divergence due to the reversed-biased run off voltage, SPICE assumes a 10^{-12} ohm resistance in parallel with each diode. Now, because our methodology for convergence is different from that of SPICE we need to assume a -10^{-12} ohm resistance in parallel with each and every diode in the circuit to cancel the effect. The second constraint in using SPICE is the reversed-biased saturation current for diodes. In SPICE I_s is fixed when a model is introduced, while in our methodology I_s is constantly changing, and different for each diode. The best solution for us is to have a modified SPICE that allows dynamic change in I_s . Similar situation exists for diode augmentation (Fig. 3). However, to run our example by the available WinSpice we had no choice but to enter the constraints manually.

Example: Consider a simple two diode circuit [10] shown in Fig. 4.

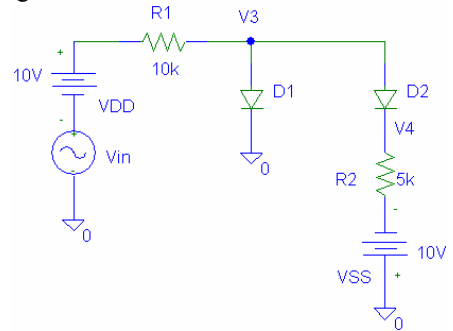


Fig. 4 - A two diode circuit.

For this example we first apply V_{DD} and remove V_{SS} from the circuit. Next, we remove V_{DD} and apply Theorem 1 to adjust the reverse biased saturation current I_s in both diodes. Figure 5 shows a WinSpice listing for this example. There are four separate circuits in this listing, running simultaneously. The first part represents the original circuit as given in Fig. 4 (some non-essential components are not shown). The second list is for the diode circuit with only V_{DD} present. Now, this source turns both diodes on with $I_{D1} = 9.089857e-4$ A and $I_{D2} = 1.979574e-05$ A. Next, we remove V_{DD} and apply V_{SS} to the circuit. The other changes that we need to do is to define two new models, TRR1 and TRR2 for the diodes with I_s' equal to I_{D1} and I_{D2} ($I_s = 10^{-15}$ A is ignored), respectively. The third circuit makes D_1 off, and this is because the new Q point on D_1 characteristic

experiences a reverse biased voltage of total $V_{D2} = -2.8525712$ V. To stop the voltage run off we augment, as we discussed earlier, a voltage source $V_{d13} = V_{D2}$ in series with D_1 , and go back to the original model TRR (D_2 takes another model TRR4). This concludes the SPICE listing.

We next test all four circuits by applying a swiping voltage source V_{in} , changing from -2 to 12 volts. Figures 6(a) and (b) show the node voltages from the first and the last circuits, namely $V(3)+2.85$ and $V(4)+3.57$ are from the original circuit, and $V(33)$ and $V(43)$ are from the last circuit with $V_{DD} = V_{SS} = 0$.

We can observe the followings:

- $V(33)$ and $V(43)$ pass through the origin, that is, no dc is present in the circuit while $V(3)$ and $V(4)$ have offset voltages equal to 2.85 and 3.57 volts, respectively.
- The diodes breakpoints appear at the same locations for both circuits, and the differences are very small and due to round off errors, as depicted in the close-up graph, shown in Fig 6(b).

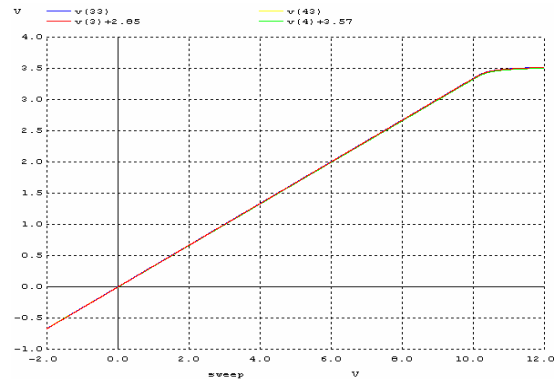
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*** The original diode circuit ***
D1 3 5 TRR
rd1 3 5 -1.0e+12
D2 3 4 TRR
rd2 3 4 -1.0e+12
R1 10 3 10k
R2 4 2 5K
Vd1 5 0 DC 0
Vdd 10 1 DC 10
Vin 1 0 0
Vss 2 0 DC -10
*
* Only Vdd is on
D11 31 51 TRR
rd11 31 51 -1.0e+12
D21 31 41 TRR
rd21 31 41 -1.0e+12
R11 101 31 10k
R21 41 21 5K
Vd11 51 0 DC 0
Vdd1 101 1 DC 10
Vss1 21 0 DC 0
*
* Only Vss is on
D12 32 52 TRR1
rd12 32 52 -1.0e+12
D22 32 42 TRR2
rd22 32 42 -1.0e+12
R12 102 32 10k
R22 42 22 5K
Vd12 52 0 DC 0
Vdd2 102 1 DC 0
Vss2 22 0 DC -10

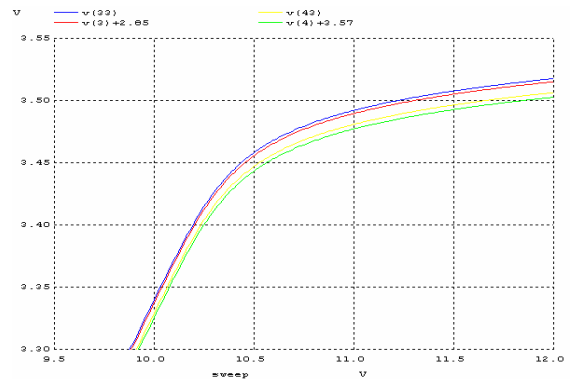
* No source
D13 33 53 TRR
rd13 33 53 -1.0e+12
D23 33 43 TRR4
rd23 33 43 -1.0e+12
R13 103 33 10k
R23 43 23 5K
Vd13 53 0 DC 2.8525712
Vdd3 103 1 DC 0
Vss3 23 0 DC 0
*
***** Spice models and macro
models *****
.Model TRR D
+ IS=1.0E-15 TT=30E-9 CJO=1E-12
VJ=.7 M=.33
***
.Model TRR1 D
+ IS=9.089857e-4 TT=30E-9
CJO=1E-12 VJ=.7 M=.33
***
.Model TRR2 D
+ IS=1.979574e-05 TT=30E-9
CJO=1E-12 VJ=.7 M=.33
***
.Model TRR4 D
+ IS=0.00128525674 TT=30E-9
CJO=1E-12 VJ=.7 M=.33
***
.probe
.dc Vin -2 12 0.01
*#run
*#plot V(3)+2.85 V(4)+3.57 V(33)
V(43)
.end

```

Fig. 5 – SPICE listing for four part circuit example.



(a)



(b)

Fig. 6 – (a) Diode circuit output responses, and (b) a close-up section.

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